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Three-Phase Reduced Switch Topologies for AC-DC Front-End and Single-Stage Converters

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A thesis submitted in partial fulfillment of the requirements for the degree in Doctor of Philosophy

THREE–PHASE REDUCED SWITCH TOPOLOGIES FOR AC–DC FRONT–END AND SINGLE–STAGE CONVERTERS

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by

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Abstract

Conventional three-phase AC-DC converters have two converter stages. They have a front-end converter that converts the input AC voltage into an intermediate DC bus voltage and a second, back-end converter that converts this DC bus voltage into the desired isolated DC output voltage. The front-end converter also performs power factor correction (PFC) and shapes the three-phase input currents so that they are nearly sinusoidal and in phase with the three-phase input voltages. This allows the AC power source to be used in the most efficient manner.

The front-end AC-DC converter is typically implemented with six switches while the back-end DC-DC converter is typically implemented with a four switch DC-DC full-bridge topology. Power electronic researchers have been motivated to try to reduce the number of switches that are used in the conventional two-stage approach in order to reduce cost and simplify the overall AC-DC converter. There are two general approaches to doing this: This first approach is to reduce the number of switches in the front-end AC-DC converter. The second approach is to combine the AC-DC converter and the DC-DC converter in a single converter so that the overall AC-DC converter can be implemented in a single converter stage that can simultaneously perform AC-DC power conversion with PFC and DC-DC power conversion.

The main focus of this thesis is on new power converter topologies that convert a three-phase AC input voltage into an isolated DC output voltage with a reduced number of switches. In the thesis, a new family of reduced switch front-end converter topologies is proposed, an example converter from this new family is selected for further study and a modified version of this topology is studied as well. In addition to these front-end converters,

two new three-phase AC-DC single-stage converters are proposed and their properties and characteristics are compared. For each new converter that is investigated in detail, its modes of operation are explained, its steady-state characteristics are determined by mathematical analysis, and the results of the analysis are used to develop a design procedure that can be used to select key components. The design procedure of each new converter is demonstrated with an example that was used in the implementation of an experimental prototype that confirmed the feasibility of the converter.

The thesis concludes by presenting that have been reached as a result of the work that was performed, stating its main contributions to the power electronics literature and suggesting future research that can be done based on the thesis work.

KEYWORDS: Three-phase rectification, AC-DC conversion, power factor correction, reduced-switch converters, multilevel converters, soft-switching, three-phase power conversion, single-stage converters.

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And last but not least, I am thankful to my loving mother Indira and to my Aunt Sandhya for the endless love that they have given me.

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Dedication

This Thesis is dedicated to my loving late-father *Indra* and mother *Indira*.

Without their love, wisdom, and guidance, I would not have the realized my goals to make my dreams come true!!!

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List of Nomenclature

C_a, C_b, C_c	Input Capacitors
C_{bus}	Dc bus capacitor
C_{fly}	Flying capacitor
C_o	Output capacitor
C_x	Auxiliary capacitor on transformer secondary side
D	Switch duty cycle
D_{o1}, D_{o2}	Output diode
D_x	Diode
f_l	Line frequency
f_r	Dominant harmonic frequency (sidebands) related to the switching frequency
f_s	Switching frequency
I_a	Line current
i_{bus}	Bus current
$i_{Ca,k}$	Instantaneous input capacitor current
i_{fb}	Full-bridge current
I_{lfr}	High frequency input ripple current in to the utility side
i_{Llk}	Instantaneous current through leakage inductor
I_{Lo}	Output inductor current
I_o	Dc output current
I_{rms}	Input rms line current
L_a, L_b, L_c	Input inductors
L_{lk}	Leakage inductance
L_o	Output inductor
L_x	Inductor
M	Output-to-input voltage conversion ratio
n	Transformer turns ratio
n_{pri}	No. of turns in the primary winding
n_{sec}	No. of turns in the secondary winding
$P_{o,max}$	Maximum output power
R	Resistor

S	Switch
T	Transformer
T_l	Line period
t_{on}	Switch On time
T_s	Switching Period
$v_{Ca,k}$	Instantaneous input capacitor voltage in k^{th} switching cycle
$V_{Ca,ave}$	Average voltage of capacitor C_a
$V_{Ca,pk}$	Peak voltage of capacitor C_a
$v_{Ca,k}$	Instantaneous voltage of C_a in k^{th} switching cycle
V_{CM}	Peak capacitor voltage
V_{Cfly}	Voltage across flying capacitor
$v_{Cx,k}$	Instantaneous voltage of C_x in k^{th} switching cycle
V_{dc}	DC voltage (source)
v_D	Voltage across diode D
V_{g1}, V_{g2}	Gate pulse of switch S_1, S_2
$v_{La,k}$	Voltage across input inductor
L_{bus}	Dc bus inductor
$v_{Cx,k}$	Instantaneous voltage across auxiliary capacitor C_x
$V_{ll,rms}$	Three-phase line-line rms voltage
v_{Lbus}	Instantaneous voltage across bus inductor
V_o	Output voltage
$v_{rec,k}$	Instantaneous output voltage of three-phase diode rectifier in k^{th} switching cycle
$V_{S,pk}$	Peak switch voltage
W_i	Total input energy
W_a	Input energy of phase A
W_o	Output energy
ω_l	Angular line frequency

List of Abbreviation

AC	Alternating current
CVM	Continuous voltage mode
DC	Direct current
DVM	Discontinuous voltage mode
FCMC	Flying capacitor multilevel converter
FFT	Fast Fourier transform
IGBT	Insulated gate bi-polar transistor
MOSFET	Metal oxide field effect transistor
NPCMC	Neutral-point connected converters
PF	Power factor
PFC	Power factor correction
PWM	Pulse width modulation
QR	Quasi-resonant
TPSSC	Three-phase single switch converter
ZCS	Zero-current switching
ZVS	Zero-voltage switching
ZVZCS	Zero-voltage-zero-current switching

Chapter 1

1 Introduction to Thesis

1.1 Introduction

Power electronic converters use active semiconductors (e.g. IGBTs) and passive power semiconductors (e.g. diodes) and passive elements (e.g. inductors and capacitors) arranged in circuit structures to convert power from the form available from a source to that required by a load. The power source may be a DC source, a single–phase AC source, or a three-phase AC source with line frequency of 50, 60 or 400 Hz. It may also be an electric battery, a solar panel, an electric generator or a commercial power supply. The source feeds the input of the power converter, which converts the input power to the required form for a load. The load may be DC or AC, single–phase or three–phase, and may or may not need transformer isolation from the power source. The power converter, therefore, can be an AC/DC converter, a DC/DC converter, a DC/AC inverter or an AC/AC converter depending on the application.

The main focus of the research in this thesis has been on three-phase AC-DC power converters. These are converters that convert a three-phase input voltage into an isolated DC output voltage. The three-phase AC voltage is typically obtained from the utility mains. Ac-DC power converters connected to the mains voltage can generate and inject current harmonics into the utility mains. Injecting current harmonics into the AC mains results in two significant consequences:

- First, because of the finite impedances of the power lines, harmonic currents generate voltage variations at the point of common coupling that other equipment on the line must tolerate.
- Second, although current harmonics do not generate real power, they must be considered in the design of power lines so that power lines must be significantly overrated lest they overheat.

As a result, regulatory bodies have imposed strict limits on the harmonics that power converter can inject into the utility mains.

To minimize the harmonics generated by power converters, power factor correction (PFC) techniques have been developed so that the generated harmonics comply with regulatory agency standards such as IEC 61000-3-2 Class A. Power factor (PF), which is a measure of how effectively the input AC source is used can be defined as

$$PF = \frac{P}{\sqrt{3}V_{ll(rms)}I_{rms}} \tag{1.1}$$

where P is the output real power, $V_{ll,rms}$ is the three-phase line-line rms voltage and I_{rms} is the input rms line. A power factor of 1 is the maximum power factor that can be achieved and represents the most efficient use of the input AC source.

AC-DC power converters implemented with PFC techniques are made to operate in such a way that their input currents are shaped so that they are sinusoidal and in phase with their respective phase voltages. Most AC-DC power converters today that are supplied by the AC mains are implemented with some sort of PFC technique and the implementation of PFC in power electronic converters is a very relevant research topic in the power electronics field.

1.2 Three-Phase Two-Stage Power Factor Correction

Typically, three-phase AC-DC power converters with transformer isolation are implemented with two converter stages that are independent of each other; a generic block diagram of a two-stage AC-DC converter is shown in Fig. 1.1. The first stage is an AC-DC conversion (rectifying) stage and the second stage is an isolated DC-DC conversion stage. A rectifier or front-end converter is used to convert the three-phase AC voltage into an intermediate DC bus voltage and is then fed to a second converter or back-end converter that converts it into the desired, isolated, DC voltage. An example two-stage converter is shown in Fig. 1.2, where the three-phase AC-DC front-end is a six-switch converter and the DC-DC back-end is a full-bridge converter. The two converter stages are discussed in more detail below.

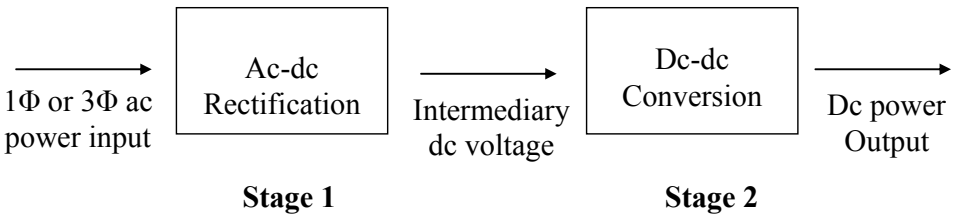


Fig 1.1: Three–phase AC–DC six switch two–stage full–bridge converter [1].

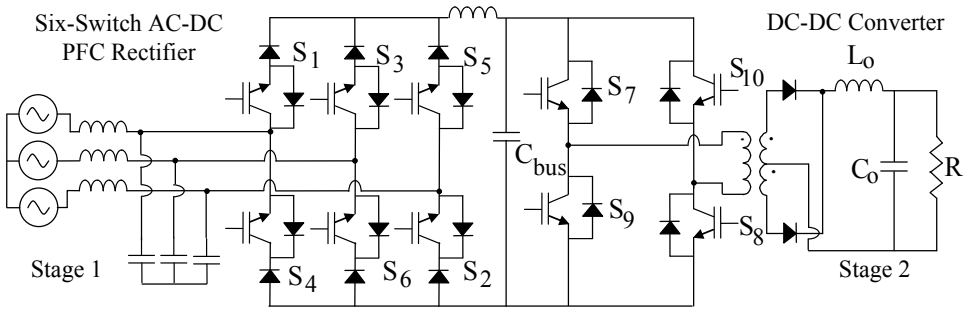


Fig 1.2 Three–phase AC–DC six switch two–stage full–bridge converter.

1.2.1 DC-DC Full-Bridge Converter

The DC-DC full-bridge converter topology shown in Fig. 1.3(a) is the standard topology that is used for higher power DC-DC power conversion (> 500 W). The converter consists of four switches (S_1 - S_4), a transformer (T), two output diodes (D_1, D_2), an inductor (L_o) and a capacitor (C_o); the load is represented as a resistor. The converter works as follows: voltage is impressed across the primary of the transformer

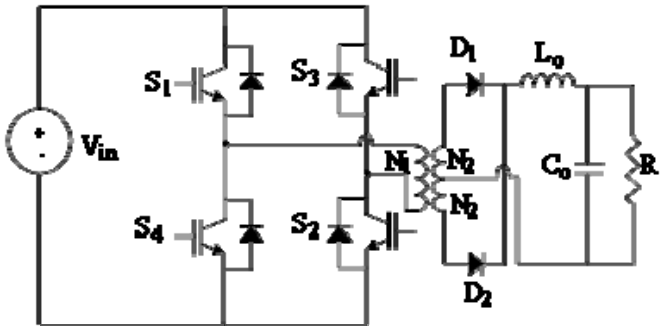


Fig 1.3(a): Three-phase AC-DC six switch two-stage full-bridge converter.

winding whenever a diagonally opposite pair of switches are on (S_1 and S_2 or S_3 and S_4); the polarity of the voltage depends on the pair of switches that is on. No voltage is impressed across the transformer primary whenever current flows through two top switches (or their body-diodes) or two bottom switches (or their body diodes). Typical switch gating signals and a typical primary voltage waveform are shown in Fig. 1.3(b).

Each converter switch is on for 50% of the switching period and there is no overlap

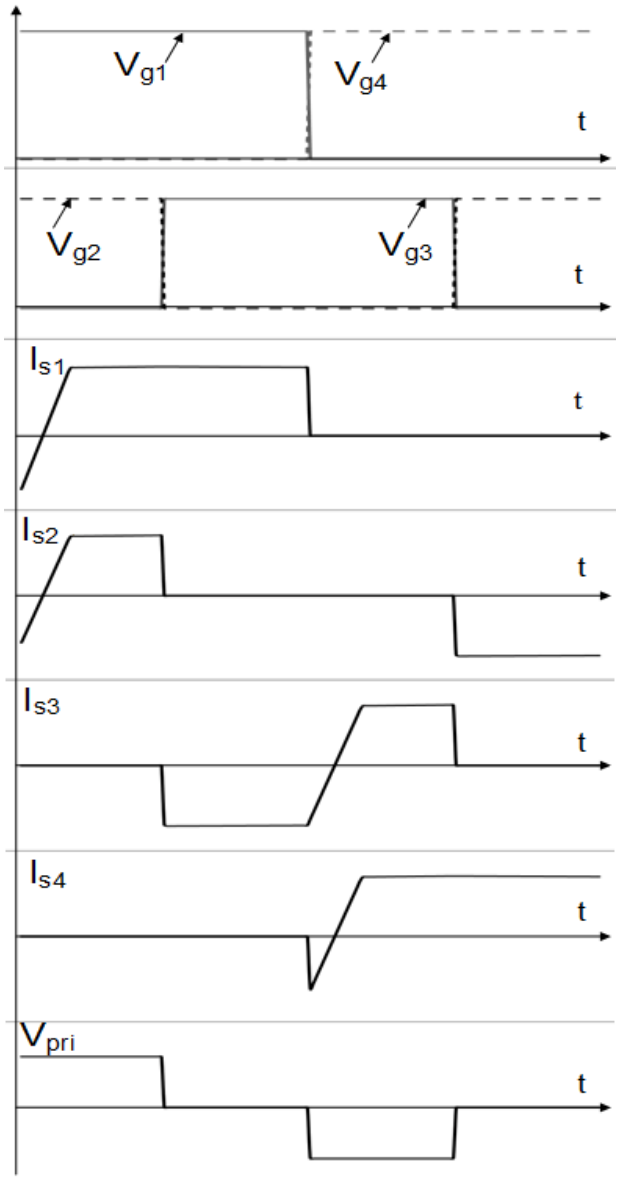


Fig 1.4(b): Phase-shift PWM switching scheme and full-bridge converter

between the gating signals of the two switches in each leg, to avoid short-circuiting. The output voltage is controlled by shifting the gating signals of the switches in one leg with respect to those of the switching in the other leg, which controls the length of time voltage is impressed across the transformer. The converter can be said to be in a power transfer mode whenever a voltage is impressed across the transformer primary and appears at the secondary, and to be in a freewheeling mode when there is no voltage across either transformer winding and current just flows ("freewheels") throughout the converter. The primary voltage waveform is an AC waveform that is stepped down or up (typically down), rectified by the two secondary output diodes, then filtered by a low-pass filter formed by L_o and C_o to produce the required output DC voltage.

1.2.2 Three-Phase AC-DC Front-End Converters

The front-end converter converts the three-phase input voltage into an intermediate DC bus voltage while simultaneously performing some sort of PFC technique to ensure an input power factor as close to unity as possible. The use of six-switch front-end rectifiers such as the one shown in Fig. 1.2 is the standard when implementing PFC in three-phase AC-DC PFC. For the front-end converter shown in Fig. 1.2, PFC is performed by sensing the three-phase input voltages and currents and then turning the converter switches on and off in an appropriate manner so that the current in each phase is nearly sinusoidal and in phase with the corresponding phase voltage. Numerous PFC schemes for three-phase front-end converters have been proposed [2]-[4], but they will not be reviewed here as they are outside the scope of this thesis.

Using six switches in the front-end converter of a two-stage AC-DC converter can be costly and complicated – especially when the associated gate drive and control circuitry and input currents sensors are considered. As a result, researchers have been motivated to find alternative methods of performing AC-DC power conversion and PFC with a converter having fewer switches. In general, most of these methods can be classified as follows:

1.2.2.1 Modular PFC Method

One alternative to the standard six-switch three-phase AC-DC rectifier is to use three separate single-phase boost PFC converter modules as shown in Fig. 1.4 [5]-[8]. Each module in Fig 1.4 is a two-stage converter consisting of PFC boost front-end converter followed by a DC-DC back-end converter to get the desired bus voltage. The main advantage is that existing single-phase modules can be used, which are popular and widely available and do not require knowledge of sophisticated three-phase control. The main disadvantages are the need to synchronize the operation of each individual module to the others, the presence of triplen harmonics due to parametric variations in the modules, and the high number of components.

1.2.2.2 Reduced Switch Front-End Converters

Several researchers have proposed front-end AC-DC converters with a reduced number of switches, less than six switches typically found in conventional front-end converters [9]-[10]. Two of the more popular converters of this type are briefly explained below.

- Four-Switch Converter - The converter shown in Fig. 1.5(a) [9] is a four switch converter that has two legs with two switches in each leg and a third leg that is made with two capacitors (C_1, C_2). The midpoint of each leg is connected to a phase of the three–phase source. The general principle behind this converter is that if the phase currents that are associated with the converter legs that have switches

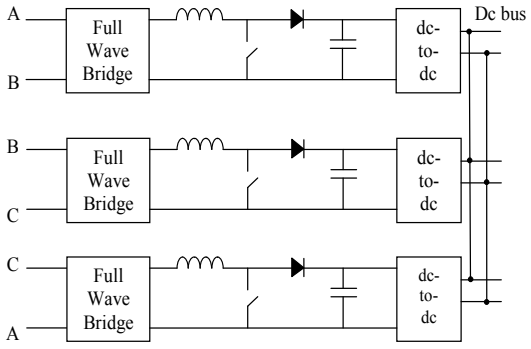


Fig 1.5: Three-phase AC-DC converter using three single-phase modules.

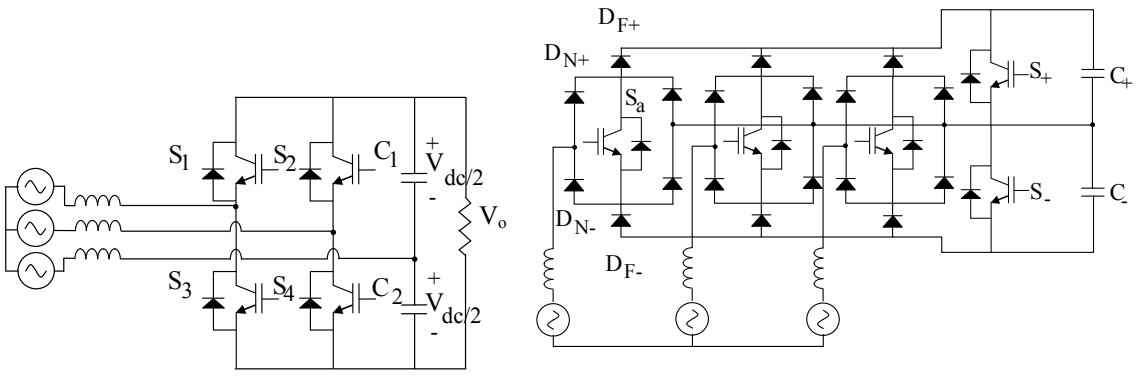
are controlled, then the third phase current will be constrained by the other two phase currents so that it too will be sinusoidal and in phase with the phase voltage.

- Vienna Rectifier - The converter shown in Fig. 1.5(b) [10] has three main power switches that are implemented with four diodes to each switch to make them bidirectional and allow current to flow through each direction. The converter can be operated like a conventional six-switch converter but with one bidirectional switch in each converter leg instead of two unidirectional switches.

Although reduced switch converters may be less expensive than six-switch converters, they require the use of control methods that are much more sophisticated than those used in conventional six-switch converters. These methods are not easy to implement and their performance merits are not clear when compared to conventional six-switch converters so that reduced switch converters are not widely used in the power electronic field.

1.2.2.3 Single-Switch Front-End Converters

For lower three-phase power applications, it is possible to perform PFC by using only a single switch [11]-[16] as the stress that is placed on the switch device is not excessive. The first such converter to be proposed was the three-phase single-switch AC-DC boost converter shown in Fig. 1.6 [11] as the front-end AC-DC converter of a two-stage converter. The converter consists of three boost inductors (L_a, L_b, L_c), three-phase diode-



(a). Four-switch front-end converter

(b). Vienna rectifier

Fig 1.6: Reduced switch three-phase AC-DC converters.

bridge, switch (*S*), diode (*D*) and a filter capacitor (*C*); an input filter is used to filter out higher frequency harmonics that are created by the converter's switching operation. The converter is simple as it only requires one switch operating with high switching frequency (> 5 kHz) and does not require any sensors to sense the input currents or any controller that is dedicated to ensure that the input voltages and currents are in phase. The converter needs just a single controller to regulate its output voltage. Although several single-switch front-end AC-DC converters have been proposed [15]-[16], the single-switch converter shown in Fig. 1.6 is by far the most popular single-switch front-end converter that is used for general applications and most other single-switch front-end converters are either variations of the converter shown in Fig. 1.6. or are limited to certain niche applications.

1.3 Three-Phase Single-Stage PFC

Although reduced switch front-end AC-DC converters can reduce the size and cost of conventional two-stage converters, two separate and independently controlled converters are still needed (Fig. 1.7). In order to reduce the cost and complexity associated with implementing two switch-mode converters, power electronics researchers have tried to combine the PFC function of the AC-DC front-end converter with the DC-DC conversion function of the full-bridge converter in a single converter [17]-[27]. Some frequently cited examples for three-phase single-stage converters (TPSSCs) are shown in Fig. 1.8. Each subfigure shows a different TPSSC topology. These converters are typically implemented with just a single controller to regulate the output voltage so that there is no controller to regulate the intermediate DC bus voltage and no controller to perform input

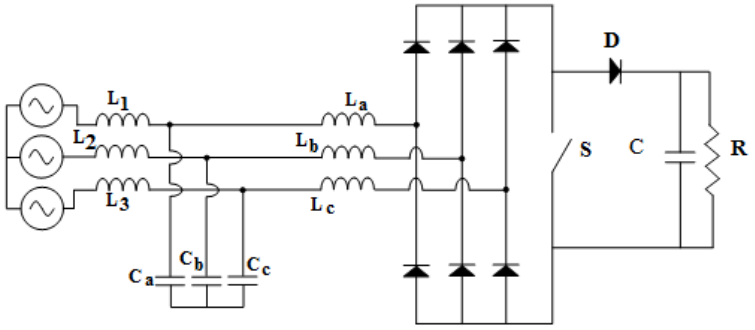


Fig 1.7: Three–phase AC–DC single–switch boost front-end converter.

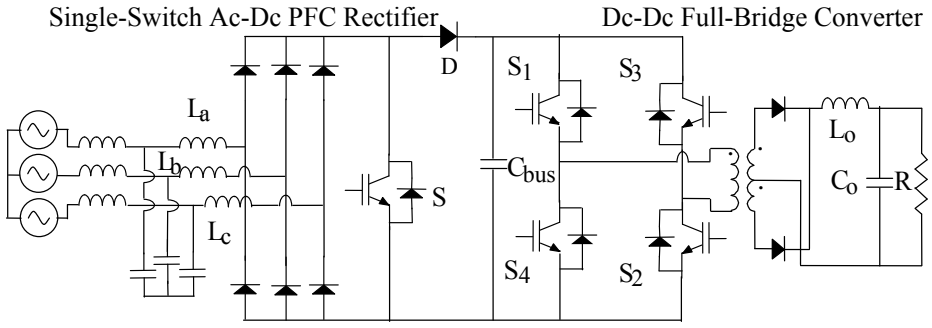


Fig 1.8: Three–phase AC–DC single–switch boost rectifier and DC–DC full–bridge converter.

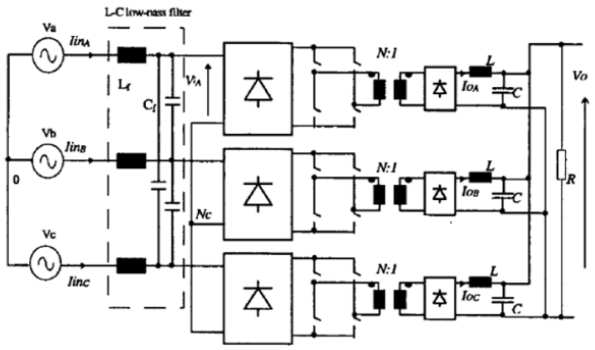
PFC; input PFC is done naturally as a function of the converter's operation.

The design of a three-phase single-stage converter is challenging because the converter must simultaneously performing both PFC and DC-DC conversion over the entire load and input range with only a single controller and without additional input current sensing and DC bus voltage control. As a result, relatively little research has been successfully done in this area and a trade-off must be made between the simplicity of single-stage converters and the better performance of more expensive two-stage converters. TPSSC that have been previously proposed have at least one of the following drawbacks:

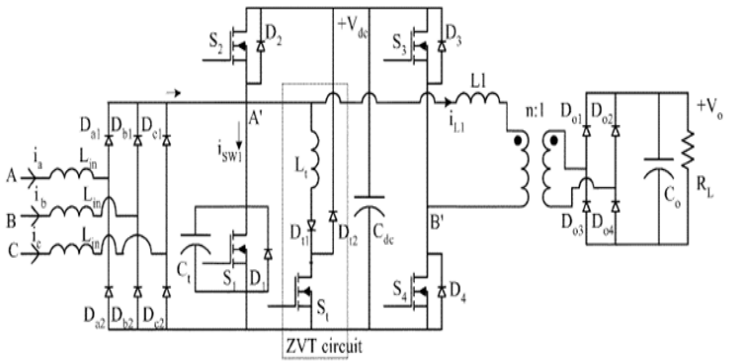
- The converter uses a three single-phase full-bridge modular approach [6] (i.e. Fig. 1.8(a)). This is expensive and it is not easy to synchronize the operation of all three converters to produce sinusoidal input currents.

- The input currents must be discontinuous in order for input power factor correction to be achieved (i.e. Fig. 1.8 (b)-(d)). Converters such those proposed in [17]-[23] incorporate the principles of the three-phase single-switch boost converter proposed in [11] into their topologies. Although an excellent input power factor may be achieved, the peak current stress of the semiconductor devices is very high.

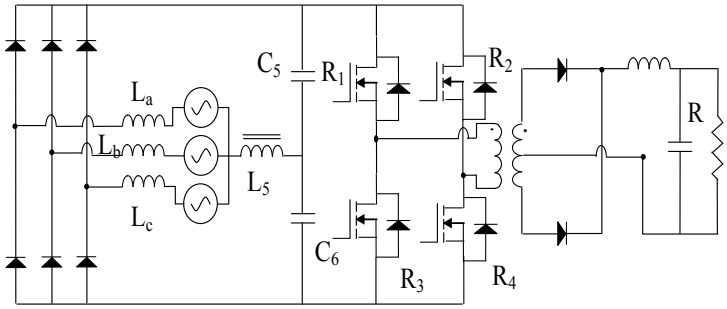
- The input currents are distorted and contain a significant amount of low frequency harmonics [21] (i.e. Fig. 1.8(c)) as the converter has difficulty performing PFC



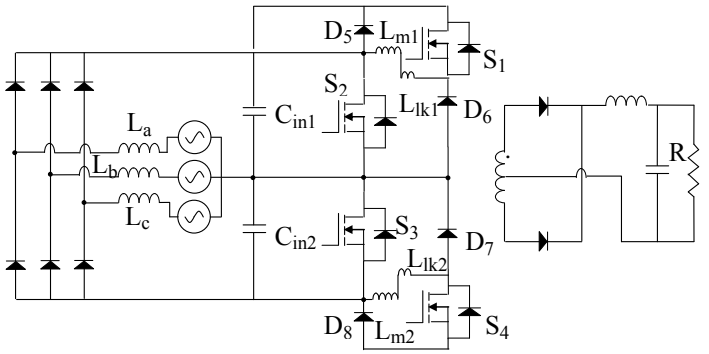
(a) [6]



(b) [18]



(c) [21]



(d) [23]

and DC-DC conversion simultaneously, thus compromising the quality of the input waveforms and PF.

- The converter must be controlled using very sophisticated techniques. This is especially true of multilevel converters [24] - [27] (i.e. Fig. 1.8(c)) where the need to balance the voltages on the split capacitors at the DC bus is critical.

1.4 Thesis Objectives

The main objectives of this thesis are as follows:

- To propose new reduced switch stress three-phase AC-DC front-end PFC converters.
- To propose new three-phase AC-DC single-stage PFC converters.
- To determine the properties and steady-state characteristics of these new converters by mathematical analysis and by using software such as MATLAB.
- To develop a design procedure for each new converter that can be used in the selection of critical converter components.
- To confirm the feasibility of each new converter with experimental results obtained from proof-of-concept prototype converters.

1.5 Thesis Outline

In addition to this chapter, this thesis comprised of six chapters. The outline of the thesis is as follows:

Chapter 2: The main focus of this chapter is to investigate the properties of converters that are based on AC-DC three-phase single-switch converters (TPSSCs), but do not have their excessive switch voltage stresses. The chapter considered two types of such converters, including a new type that has not been previously considered. It is shown how new converters with reduced switch stresses can be synthesized from a TPSSC and the peak voltage switch stresses of the switches in these new converters are considered.

Chapter 3: An example converter from the new Neutral point connected multilevel converter family is considered for further examination. In this chapter, the operation of the example converter is explained in detail, its steady-state properties and characteristics are determined by mathematical analysis, and the results of the analysis are used to establish a design procedure for the selection of key component values. The design procedure is demonstrated with an example and the feasibility of the new converter is shown with experimental results that were obtained from a prototype converter that was designed according to the design example.

Chapter 4: A technique to decrease the power losses that are created by the turn on and off of the converter in Chapter 3 is proposed in this chapter. In this chapter, it is explained how so-called soft-switching techniques can reduce these power losses and one such technique is chosen for further study, as implemented in the converter of Chapter 3. this paper. Similar to Chapter 3, the operation of this new converter is explained and analyzed and a design procedure is developed and demonstrated with an example. Experimental results that confirm the feasibility of the converter are also presented.

Chapter 5: The main objective of this chapter is to examine the operation of a buck-based, three-phase, single-stage AC-DC full-bridge converter. In the chapter, the operation of this fundamental converter is explained and analyzed, and a procedure for the design of its key components is derived and demonstrated with an example. The performance and characteristics of the converter are shown with experimental results that have been obtained from a prototype and general concluding remarks comparing buck-based and boost-based, three-phase, single-stage AC-DC full-bridge converters are made.

Chapter 6: This chapter is a continuation of the work presented in Chapter 5, as its main focus is a comparison of the performance and characteristics of the converter proposed in Chapter 5 with those of a modified version of the same converter. In this chapter, the operation, design and the features of the modified version are briefly explained and the two converters are compared in terms of parameters such as input PF, switch stresses and efficiency.

Chapter 7: The contents of the thesis are summarized, the conclusions that have been reached as a result of the work performed in thesis are presented, and the main contributions of the thesis are stated. The chapter concludes by suggesting potential future research that can be done based on the thesis work.

Chapter 2

2 Three-Phase Multilevel Front-End Converters

2.1 Introduction

Three-phase, single-switch AC-DC converters such as the ones discussed in Section 1.6 of the previous chapter are a simple and inexpensive solution for lower power applications that require three-phase input power as they require only a single power switch and can be implemented without using sophisticated control methods or input current sensing. The main drawback that has limited the widespread use of these converters is the peak voltage stress that must be placed on the main switching device. This peak voltage stress can be reduced if the single converter switch is replaced by two switches in a multilevel structure that exposes these devices to less peak voltage stress.

In this chapter, two types of multilevel converters are discussed – flying capacitor multilevel converters and neutral point connected multilevel converters. Most of the converters examined in this chapter have never been presented elsewhere. Flying capacitor multilevel converters (FCMCs) are usually used for DC-DC or DC-AC inverter applications whereas in the thesis they were synthesized for three-phase AC-DC applications. Furthermore, except for the boost neutral point connected multilevel converter (NPCMC), the other NPCMCs have not been introduced to the best of the author's knowledge.

Topologies for both types of converters are presented, the conversion from a single-switch structure to a multilevel structure is shown, and the peak switch stresses of the converter switches in each type of multilevel converter structure is examined.

2.2 Review of Operation of Basic Three-Phase Single-Switch Converters (TPSSCs)

Three-phase single-switch converters (TPSSCs) such as the one shown in Fig. 2.1 are based on DC-DC converters and are the result of replacing the input DC source with a three-phase AC source and diode bridge. There are six fundamental DC-DC converters in

the power electronics literature: buck, boost, buck-boost, Ćuk, Zeta and Sepic. When the DC source is replaced by a three-phase AC source and diode bridge as shown in Fig. 2.1, six fundamental TPSSCs can be formed. The power factor correction (PFC) of any of these TPSSCs can be done without sensing any input parameter and an additional controller, as it can occur automatically as a function of the converter's natural switching operation. The converter can operate like a DC-DC single-switch converter with a switch duty cycle (D) that can be considered to be fixed throughout the input line cycle.
The six fundamental converters can be divided into two main groups:

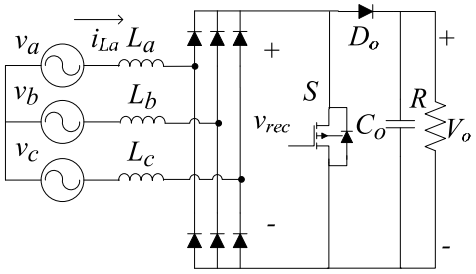
- Converters with an inductive input filter (Boost, Ćuk and Sepic)
- Converters with a capacitive input filter (Buck, Buck-boost and Zeta)

The converters with an inductive input filter ensure the input inductor currents (e.g. i_{La}) rise and fall in every switching cycle whereas the converters with a input capacitive filter ensure the capacitor voltages (e.g. v_{Ca}) rise and fall. The fundamental operation of an example converter of each group is reviewed below.

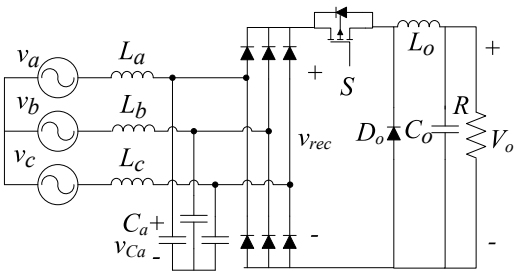
2.2.1 Converters with an Inductive Input Filter

The single-switch boost converter shown in Fig. 2.1(a) is an example of a TPSSC with an inductive input filter. The converter operates as follows: The currents in all three input inductors rise whenever the switch (S) is on and fall to zero whenever the switch is off. This is shown in Fig. 2.2(a), where i_{La} is the current of input inductor L_a that rises from zero to a peak value determined by the instantaneous phase A voltage when S is on ($t_{on} = DT_s$). After S is turned off ($t_{off} = T_s[1-D)$], i_{La} decreases from its peak value to zero and remains at zero until S is turned on again. The input currents are discontinuous and are a train of triangular pulses whose peaks are bounded by a sinusoidal envelope. This allows a nearly sinusoidal average current (current without high frequency ripple) to be achieved in all three phases. The Ćuk (Fig. 2.1(b)) and Sepic (Fig. 2.1(c)) converters are the other two TPSSCs with an inductive input filter and their input currents can be made to be sinusoidal in the same way as the boost converter.

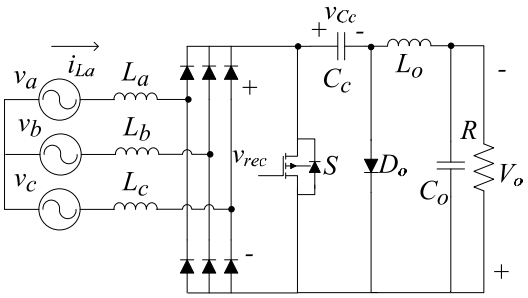
Inductive Input Filter ***Capacitive Input Filter***



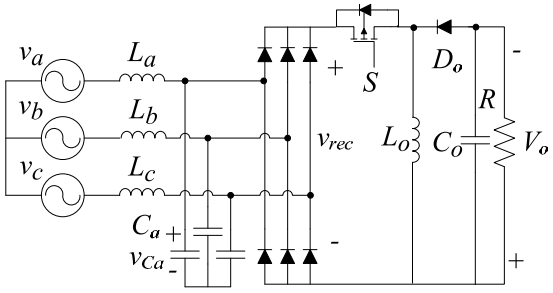
(a) Boost converter



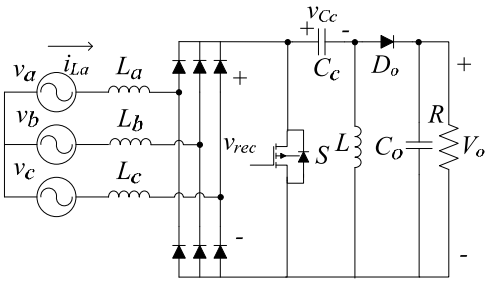
(d) Buck converter



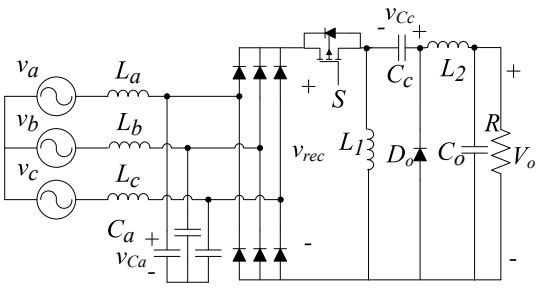
(b) Ćuk converter



(e) Buck-boost converter



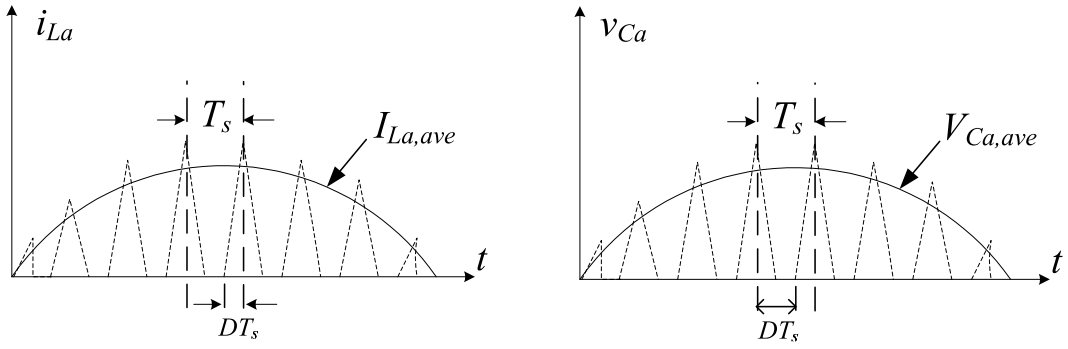
(c) Sepic converter



(f) Zeta converter

Fig 2.1: Three-phase single-switch PFC converters.

At the DC side of the boost converter, after the input diode bridge, the converter behaves as a typical DC-DC boost converter - the input inductors charge using the line currents when *S* is on and feed the load when *S* is off [1]. When *S* is off, output diode D_o in Fig. 2.1(a) is forward biased, and as a result the output voltage (V_o) is placed across *S*;



(a) (b)

Fig 2.2: (a) Discontinuous input inductor current (b) Discontinuous input capacitor voltage.

thus the peak boost converter switch voltage is stress $V_{S,pk} = V_o$. The peak switch voltages of the other TPSSCs with input inductive filter are given in Table 2.1.

2.2.2 Converters with a Capacitive Input Filter

The single-switch buck converter shown in Fig. 2.1(d) is an example of a fundamental TPSSC with a capacitive input filter. The converter operates as follows: When the switch (S) is off, each of the three input capacitors (C_a, C_b, C_c) are charged to a level that is proportional to the input line-to-line voltage that is placed across it. When S is turned on, each input capacitor is completely discharged and remains at zero until S is turned off again. The rise and fall of an input capacitor voltage is shown in Fig. 2.2(b), where v_{Ca} is the instantaneous voltage of C_a – the input capacitor for phase A - and $V_{Ca,ave}$ is the average value (voltage without the high frequency ripple) of the discontinuous voltage v_{Ca}. An excellent input power factor (PF) can be achieved if the converter is made to operate with discontinuous input capacitor voltages.

Doing so ideally causes these voltages to be sinusoidal with high frequency components that are blocked by the input inductors so that the input phase currents are also sinusoidal with few if any high frequency components. This is because the voltage is a train of triangular pulses whose peaks are bounded by a sinusoidal envelope. The buck-boost [Fig. 2.1(e)) and Zeta [Fig. 2.1(f)] converters are the other two fundamental

Table 2.1: Peak switch voltage stress equations for TPSSCs.

Converter	Equation
Boost	$V_{S,pk} = V_o$
Ćuk	$V_{S,pk} = V_{Cc,pk}$
Sepic	$V_{S,pk} = V_{Cc,pk} + V_o$
Buck	$V_{S,pk} = \sqrt{3} v_{Ca,pk}$
Buck-boost	$V_{S,pk} = \sqrt{3} V_{Ca,pk} + V_o$
Zeta	$V_{S,pk} = \sqrt{3} V_{Ca,pk} + V_{Cc,pk} - V_o$

TPSSCs with a capacitive input filter. The input capacitor voltages of both these converters can be shaped so that they are discontinuous and bounded by a sinusoidal envelope just like the buck converter.

While the input capacitors are being charged and discharged, the output section of the converter operates in the exact same manner as a standard DC-DC buck converter [1]. The peak voltage stress of S in the buck converter equals the line-line voltage of input capacitors. $V_{S,pk} = \sqrt{3} v_{Ca,pk}$, where $V_{Ca,pk}$ is the peak phase voltage of C_a. The peak switch voltages of the other TPSSCs with input capacitive filter are given in Table 2.1.

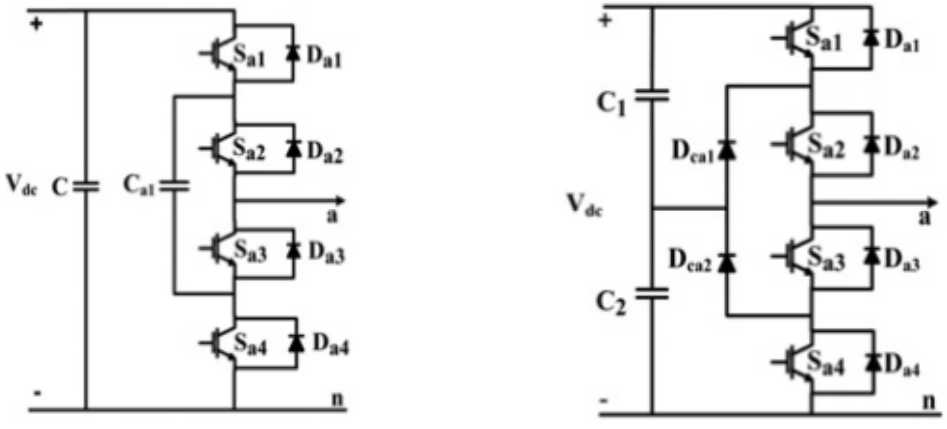
2.3 Multilevel Three-Phase Reduced-Switch Converters

The main power switch in all six fundamental three-phase AC-DC SSCs is exposed to high peak voltages. This peak switch voltage stress ($V_{S,pk}$) can be reduced if the switch is replaced by some sort of two-switch multilevel structure. Multilevel converters have topology structures that limit the voltage stresses that their switches are exposed to half the DC bus voltage of conventional two-level converters (so-called because their switches are either on or are exposed to the full bus voltage) due to the placement and connection of the components. These converters are widely used in high voltage, low switching frequency applications. They limit the switch peak voltage stress by using two bulk capacitors across the DC bus instead of one so that the midpoint of the bulk capacitors, which is half the DC bus voltage, can be used as a connection point in the converter.

Two well-known multilevel converter types are shown in Fig. 2.3. In a flying capacitor multilevel converter [Fig. 2.3(a)], the voltage across C_{a1} is half the DC bus voltage $V_{dc}/2$ and each switch is either exposed to the voltage across C_{a1}, or the difference between the bus voltage and this voltage, with the difference being $V_{dc}/2$. In a diode clamped multilevel converter [Fig. 2.3(b)] the DC bus voltage is shared by the two bulk capacitors C_1 and C_2. As a result, only a voltage across one of the capacitors is applied across a switch when it is off so that its peak voltage stress is $V_{dc}/2$.

2.4 Multilevel Converters with Flying Capacitor

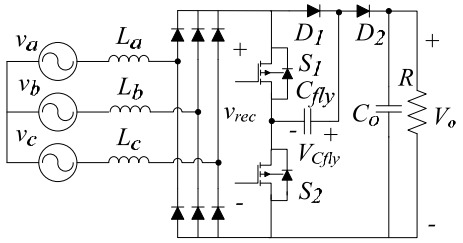
The peak voltage stress of a switch in a TPSCC can be reduced if the main switch is replaced by a flying capacitor structure like the one shown in Fig. 2.3(b). This is shown in Fig. 2.4 for all six fundamental DC-DC converters with the "flying capacitor" designated as C_{fly}. The flying capacitor structure is popular in DC-DC multilevel converters [28]-[30] and it is simple to convert a fundamental TPSSC into a flying capacitor multilevel converter (FCMC). The steps that need to be taken to perform this conversion are demonstrated in Fig. 2.5 for a Ćuk FCMC (example of a converter with an inductive input filter) and Fig. 2.6 for a buck-boost FCMC (example of a converter with a capacitive input filter) and are as follows:



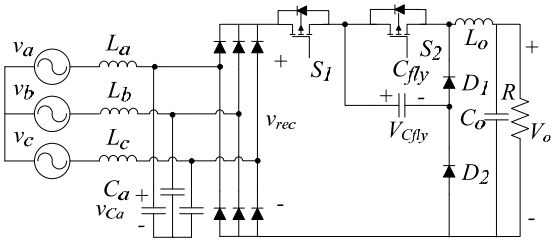
(a). Flying capacitor (b). Diode clamp

Fig 2.3: One leg of two-level multilevel converters.

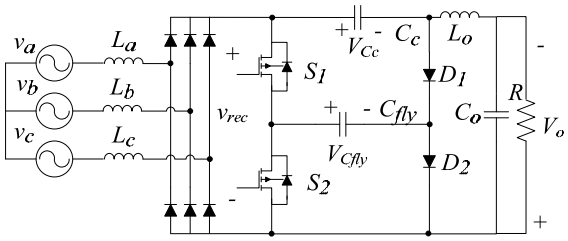
Inductive Input Filter ***Capacitive Input Filter***



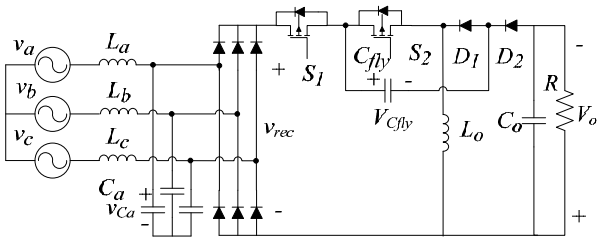
(a) Boost converter



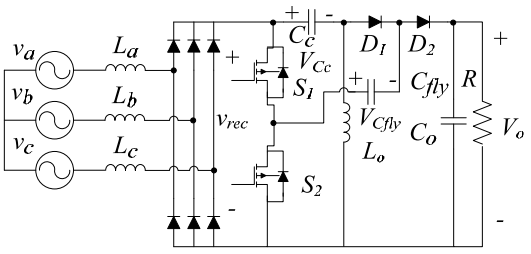
(d) Buck converter



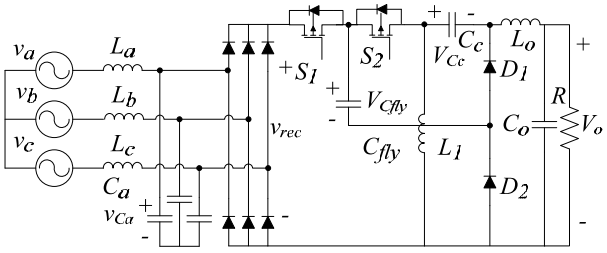
(b) Ćuk converter



(e) Buck-boost converter



(c) Sepic converter



(f) Zeta converter

Fig 2.4: Multi-level reduced switch converters with a flying capacitor.

- **Step 1**: Add a second switch in series with the main converter switch (shown as *S* in Figs. 2.5(a) and 2.6(a)), as shown in Figs. 2.5(b) and 2.6(b). There are now two main switches, S_1 and S_2.

- **Step 2**: Add a second diode in series with the main converter diode shown as D_o in Figs. 2.5(a) and 2.6(a), as shown in Figs. 2.5(c) and 2.6(c). There are now two main diodes, D_1 and D_2.

- **Step 3**: Add a bulk capacitor C_{fly} to the converter. Connect one end of C_{fly} to the midpoint of the two main power switches and the other end to the midpoint of the two main converter diodes (between D_1 and D_2), as shown in Figs. 2.5(d) and 2.6(d).

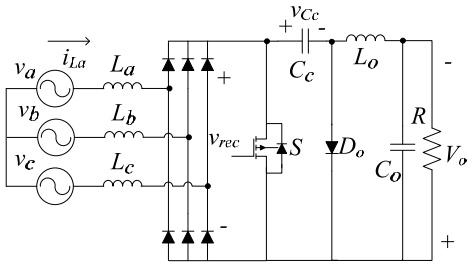
2.5 Converters with Neutral Point Connection

Although the peak voltage stress of each switch in each FCMC converters is less than that of a switch in its TPSSC counterpart, the peak voltage switch stresses can still be high and can be uneven, with the exception of the boost converter, as shown in Table 2.2. Moreover, the peak switch voltage stress in a FCMC is dependent on the voltage across the flying capacitor C_{fly}, V_{Cfly}, which can vary with load. As a result, devices with high voltage ratings may still need to be used when implementing FCMCs.

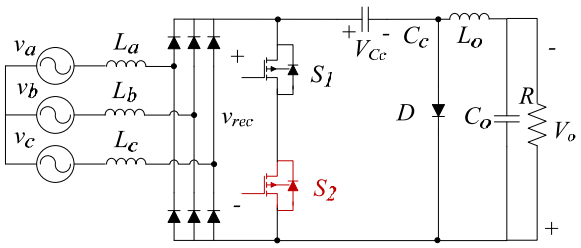
Another approach to synthesizing multilevel converters from fundamental TPSSCs is proposed here and a new family of three-phase front-end AC-DC multilevel converters can be developed. The approach is based on the connection of a neutral-point of a three-phase input capacitor filter to the general DC-DC structure and is proposed in this section. In the case of converters with capacitive input filters [Figs. 2.1(d)-(f)] such a neutral point is inherent in the converter. In the case of converters with inductive input filters [Figs. 2.1(a)-(c)], additional filtering is required to filter out high frequency harmonics so that additional input capacitors are needed and it is from these additional input capacitors that a neutral point can be created for the conversion of a single-switch topology into a multilevel neutral point topology [22]-[25].

Table 2.2: Peak switch voltage stress equations for FCMCs.

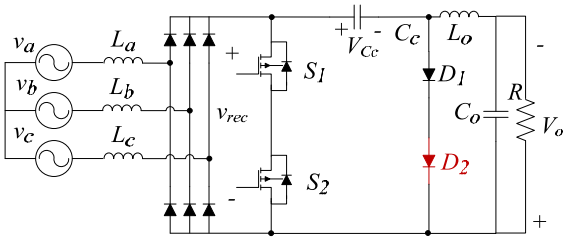
Converter	Equation
Boost	$V_{S,pk} = V_o/2$
Ćuk	$V_{S1,pk} = V_{Cc,pk} - V_{Cfly}$, $V_{S2,pk} = V_{Cfly}$
Sepic	$V_{S1,pk} = V_{Cc,pk} + V_{Cfly} - V_o$, $V_{S2,pk} = V_{Cfly} + V_o$
Buck	$V_{S1,pk} = V_{rec,pk} - V_{Cfly} = \sqrt{3} * V_{Ca,pk} - V_{Cfly}$, $V_{S2,pk} = V_{Cfly}$
Buck-boost	$V_{S1,pk} = V_{rec,pk} + V_o - V_{Cfly}$, $V_{S2,pk} = V_{Cfly}$
Zeta	$V_{S1,pk} = V_{rec,pk} + V_o - V_{Cc,pk}$, $V_{S2,pk} = V_{Cc,pk} - V_{Cfly}$



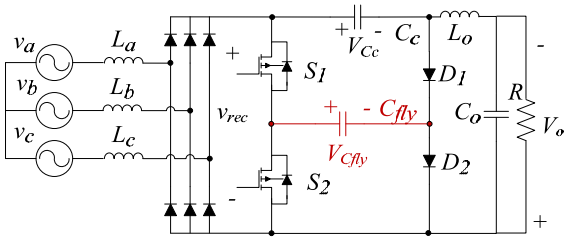
(a) Single-switch Ćuk converter



(b) Step 1

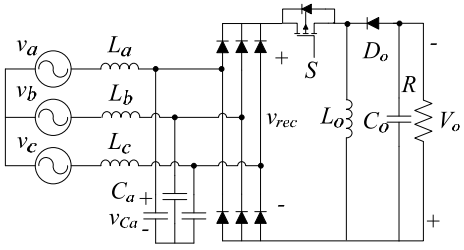


(c) Step 2

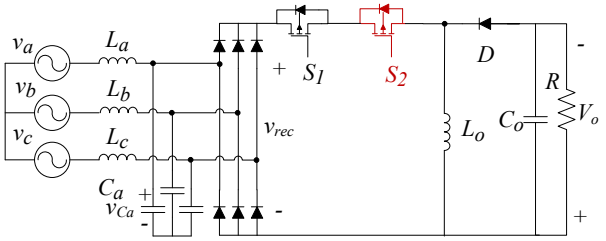


(d) Step 3

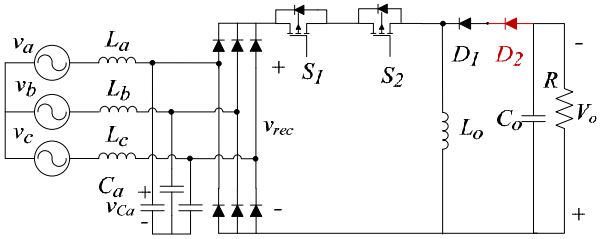
Fig 2.6: Synthesis of an example flying capacitor multilevel converter - Ćuk FCMC.



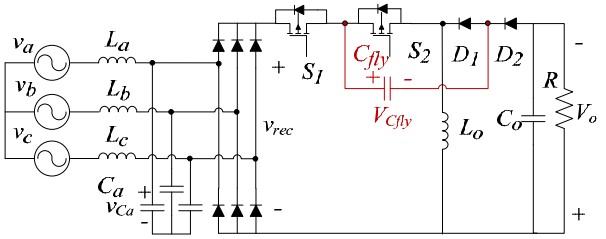
(a) Single-switch buck-boost converter



(b) Step 1



(c) Step 2



(d) Step 3

Fig 2.5: Synthesis of an example flying capacitor multilevel converter – Buck-boost FCMC.

Multilevel topologies for the six fundamental converters based on the use of the neutral point of the input capacitors are shown in Fig. 2.7. For the case of the converters with input inductor filter such as the boost, Ćuk and Sepic [Figs. 2.7(a)-(c)], it can be seen that the artificially created neutral point (x) of the additional input capacitors is connected to a midpoint that is created when two power switches are connected in series. For the case of the converters with capacitive filter such as the buck, buck-boost and Zeta [Figs. 2.7(d)-(f)], it can be seen that the natural neutral point (x) of the input capacitors is connected to a midpoint that is created when two power diodes are connected in series.

The steps that need to be taken to convert a TPSSC into a NPCMC are shown in Fig. 2.8 for a Ćuk NPCMC (example of a converter with an inductive input filter) and Fig. 2.9 for a buck-boost NPCMC (example of a converter with an capacitive input filter). The steps are as follows:

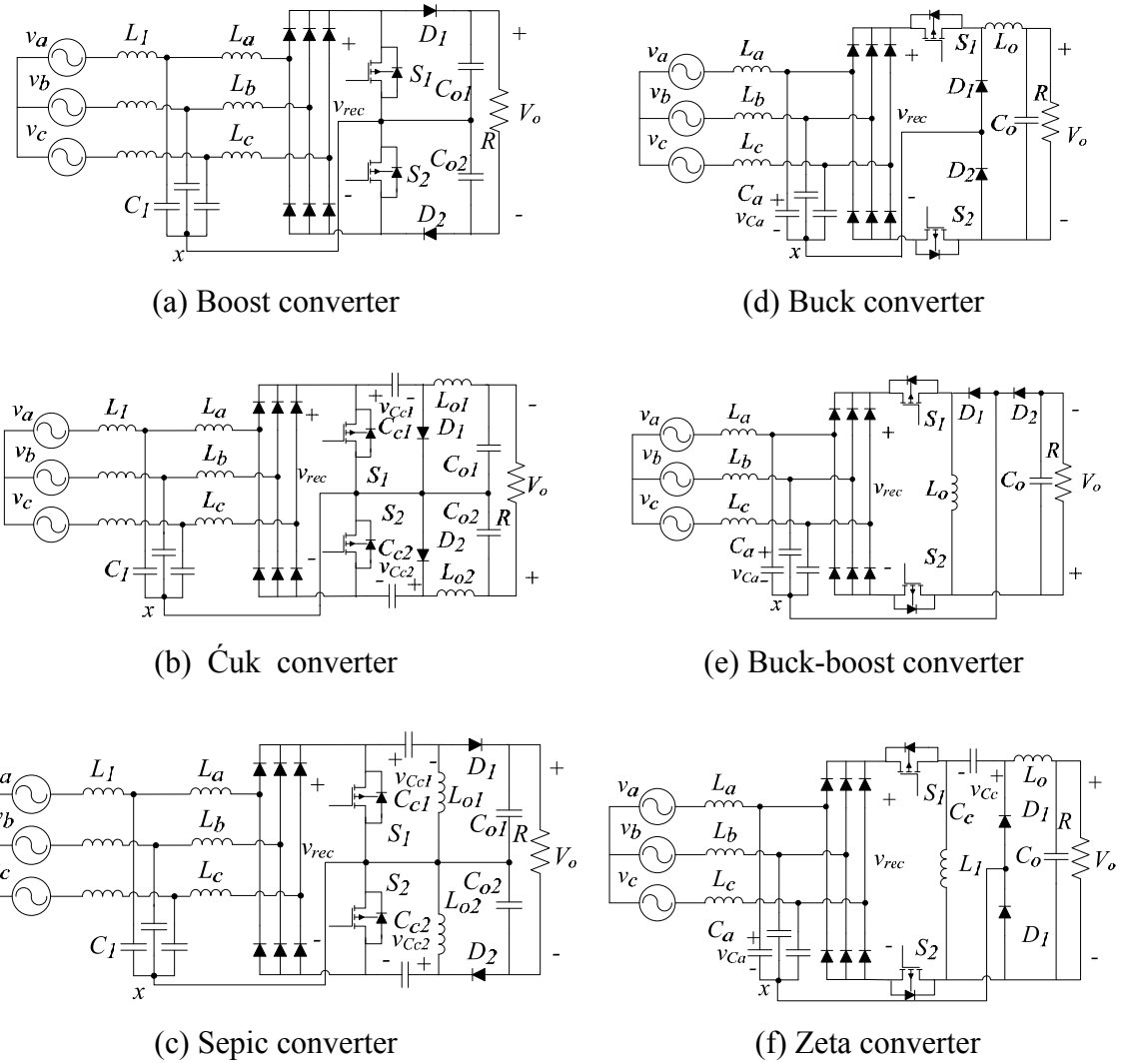
- **Step 1**: Add a second switch in series with the main converter switch (shown as S in Figs. 2.8(a) and 2.9(a)), as shown in Figs. 2.8(b) and 2.9(b). There are now two main switches, S_1 and S_2.

- **Step 2**: Add a second diode in series with the main converter diode (shown as D_o in Figs. 2.8(a) and 2.9(a)), as shown in Figs. 2.8(c) and 2.9(c). There are now two main diodes, D_1 and D_2. Also distribute the required capacitances, e.g. $C_o = C_{o1} + C_{o2}$, $C_c = C_{c1} + C_{c2}$, as shown in Figs. 2.8(c) and 2.9(c)

- **Step 3**: Connect the natural neutral point of the capacitive filter converters to the mid-point of the switches and to the mid-point of the diodes as shown in Figs. 2.8(d) and 2.9(d). In case of the inductive filter converters create an artificial neutral point by adding a capacitive filter to the input and then connect that to the mid-point of the switches, the diodes and output capacitors.

For the converters shown in Figs. 2.7(a)-(c), since the switch stress is mainly dependent on the output voltage (V_o), it can be reduced by splitting the output capacitor (C_o) so the switch stress is dependent on $V_o/2$. For the converters shown in Figs. 2.7(d)-(f), since switch stress is mainly dependent on the input capacitor voltages, it can be

Inductive Input Filter ***Capacitive Input Filter***



(a) Boost converter (d) Buck converter

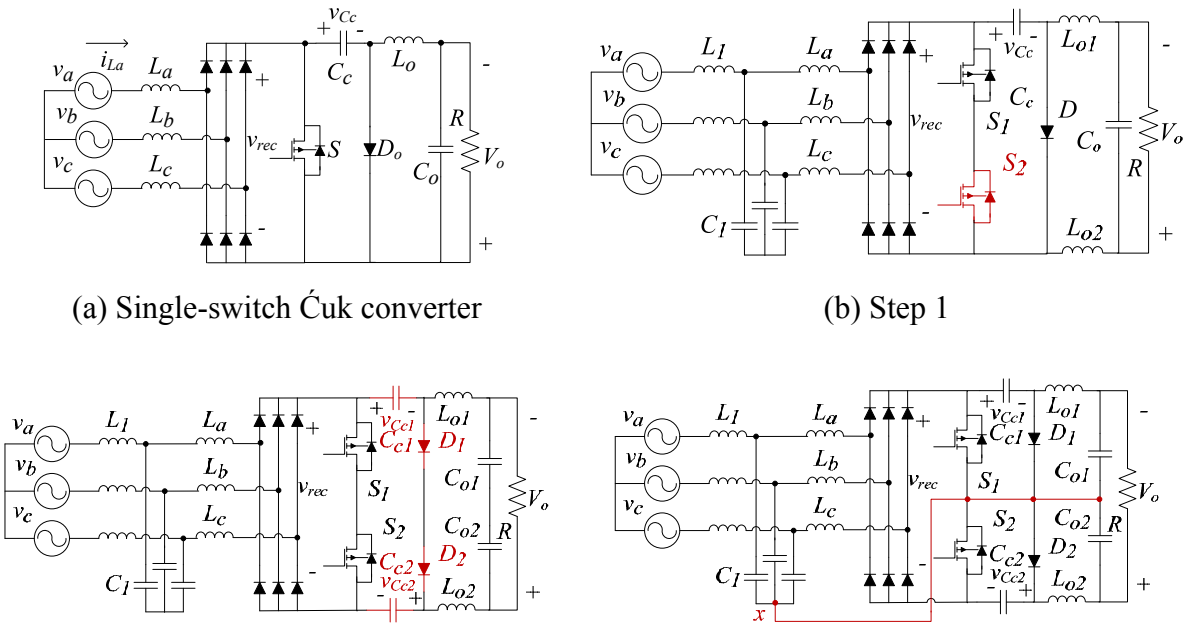
(b) Ćuk converter (e) Buck-boost converter

(c) Sepic converter (f) Zeta converter

Fig 2.7: Multi-level reduced switch converters with neutral point connection.

reduced by ensuring that a main power switch is exposed to line-neutral input capacitor voltages instead of line-line voltage as in Figs. 2.1(d)-(f), which results in a voltage stress reduction by a factor of √3.

The peak voltage stresses of the switches in a NPCMC are shown in Table 2.3. It can be seen that unlike the peak voltage switch stresses shown in Table 2.2, they are evenly



(a) Single-switch Ćuk converter

(b) Step 1

(c) Step 2

(d) Step 3

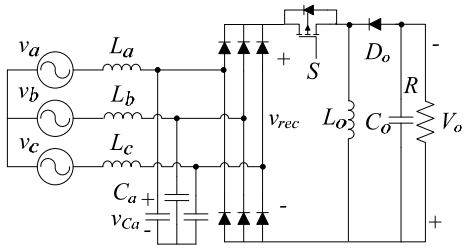
Fig 2.8: Synthesis of an example flying capacitor multilevel converter - Ćuk NPCMC.

distributed among the two switches in the converter and they are considerably less than those of a switch in a TPSSC, shown in Table 2.1.

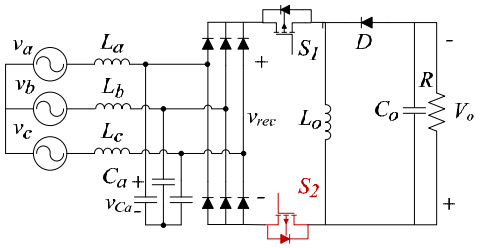
2.6 Conclusion

Three-phase AC-DC power conversion is typically done using six-switch circuit structures. An attractive way of reducing the cost, size, and complexity of such converters for lower power applications is to use single-switch converters. The peak voltage stress of the main power switch in these converters, however, is excessive, and makes these converters impractical for most applications. It is to reduce the voltage stress of this switch that multilevel circuit structures were investigated in this chapter.

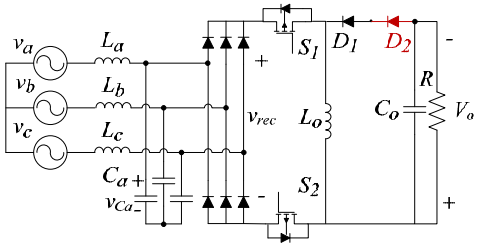
Two types of multilevel converter structures were investigated in this chapter – a family of flying capacitor multilevel converters (FCMCs) and a family of new neutral-point connected converters (NPCMCs). Since three-phase single-switch converters (TPSSCs) are based on the basic DC-DC topologies – boost, buck, buck-boost, Ćuk, Zeta, Sepic – and there are six such topologies, FCMCs and NPCMCs that are based on



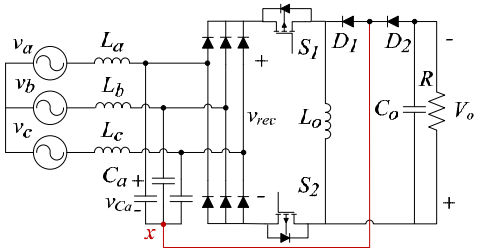
(a) Single-switch buck-boost converter



(b) Step 1



(c) Step 2



(d) Step 3

Fig 2.9: Synthesis of an example flying capacitor multilevel converter - Buck-boost NPCMC.

each basic topology were presented. The steps needed to convert a TPSSC into its FCMC and NPCMC counterparts were presented and it was explained that the peak voltage stresses of the switches in a FCMC are generally uneven except for those of a FCMC boost converter, while the peak voltage switch stress of the switches in a NPCMC are equal and approximately half those of a switch in its counterpart TPSSC.

Chapter 3

3 A Novel Three-Phase Neutral Point Connected Buck-Boost AC-DC Converter

3.1 Introduction

In Chapter 2, two types of three-phase reduced switch multilevel converters that are based on three-phase single-switch AC-DC converter were discussed – a family of flying capacitor multilevel converters (FCMCs) and a new family of neutral point connected multilevel converters (NPCMCs). In this chapter a candidate converter, the buck-boost NPCMC [Fig. 2.5(e)], is selected as an example converter to further study the operation, properties and characteristics of the new family of NPCMCs. Other reasons for selecting this particular converter for further study are that it can step up and step down voltage (since it is a buck-boost converter). A fair amount of investigation has been done on three-phase AC-DC step-up converters with an inductive input filter and step down converters with a capacitive input filter; however, there is no literature available about step-up converters with capacitive filter. Also, the candidate converter is the simplest and thus the most practical out of the four converters that can step up and step down the voltage, the others being the Ćuk, Sepic and Zeta converters.

In this chapter, the steady-state operation of the buck-boost NPCMC converter for both voltage step-down (buck) and voltage step-up (boost) operation is explained in detail and the converter's steady-state characteristics are determined by mathematical analysis. Based on the results of the analysis, a procedure that can be used in the design of the converter's key components is developed and then demonstrated with an example. The feasibility of the proposed converter is confirmed with results obtained from an experimental prototype.

3.2 Operation of the Proposed Converter

The proposed buck-boost NPCMC is shown in Fig. 3.1(a). It can be seen that the input three-phase LC filter is followed by a three-phase diode bridge. On the DC side there are two switches (S_1 and S_2), two output diodes (D_{o1} and D_{o2}), output filter inductor (L_o),

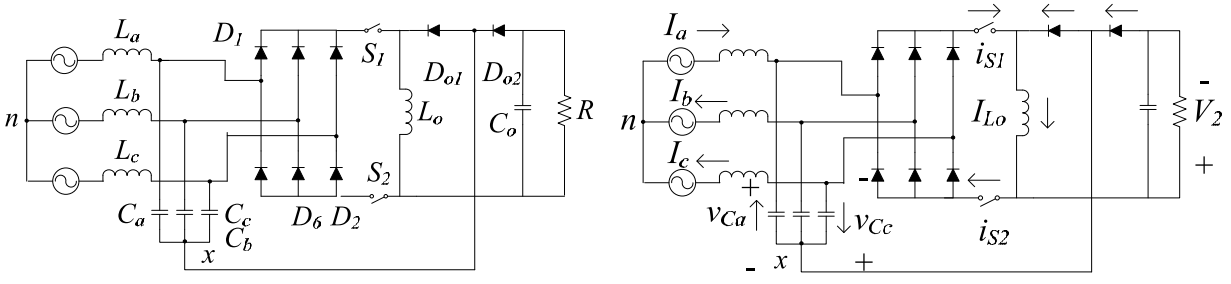
output filter capacitor (C_o) and resistive load R. The common point of the input capacitors or the neutral point (x) is connected between the two output diodes.

Input power factor correction (PFC) is performed in a way similar to that of a three-phase single-switch converter with a capacitive input filter - by the appropriate charging and discharging of the input capacitors, as explained in Section 1.7.2 [33]-[35]. The connection between x and mid-point of the diodes ensures the switch voltage stress is limited to the peak value of the input capacitor phase voltage, which helps reduce peak voltage switch stress.

The proposed buck-boost converter steps-down the input voltage or operates as a buck converter when its switch duty cycle, $D < 0.5$. The converter steps-up the input voltage or operates as a boost converter when $D > 0.5$. This section describes the operation of the proposed converter when $D < 0.5$ and $D > 0.5$. Fig. 3.1(b) indicates the reference current and voltage directions for the most important components. The equivalent circuit diagrams for the proposed converter steady-state operation when $D < 0.5$ and $D > 0.5$ are given in Figs. 3.2 and 3.4 and the typical waveforms of the two operations are given in Figs. 3.3 and 3.5 respectively.

The following assumptions are made to simplify the modal equations for the steady-state operation of the converter:

- The line frequency (f_l) is small with respect to the switching frequency (f_s); thus the input side voltages and currents are considered as constants during a switching



(a). Circuit diagram (b). Current and voltage reference directions.

Fig 3.1: Proposed three-phase AC-DC two-switch NPCMC.

period ($T_s = 1/f_s$).

- The input filter capacitors are considered to have equal values $C_a = C_b = C_c = C$. Similarly, all three input inductors are of equal value such that $L_a = L_b = L_c = L$.
- It is assumed that C is small and there is sufficient current in the DC side to discharge the input capacitors completely during a switching cycle, throughout the line cycle so that they operate in discontinuous voltage mode (DVM) as described in Section 1.7.2.
- The output capacitor C_o and the load resistor R are combined and considered as a DC voltage source (V_2) and the output inductor current is considered as a DC current $I_{Lo,k}$ with negligible ripple.
- Due to the symmetry of a three-phase system, it is sufficient to consider only $\pi/6$ of the line cycle [31]. The equations derived below are found for a switching cycle k in the line cycle for the interval $\omega_l t \; \varepsilon \; [\pi/3, \pi/2]$ where $V_{a,k} = V_1$, $V_{b,k} = V_{c,k} = -V_1/2$ and V_1 being the peak phase voltage. It should be noted that the equations can be generated by starting from any switching cycle; this particular cycle was selected to reduce redundant equations.

3.2.1 $D < 0.5$ [Buck mode of operation]

Prior to $t = t_0$, both S_1 and S_2 are off and the input capacitors are charged by the input line currents. While this is happening, the current in L_o ($I_{Lo,k}$) is freewheeling in the DC side of the converter.

Mode 1 ($t_0 < t < t_1$), [Fig. 3.2(a)]:

At $t = t_0$, S_1 is turned on and the line current, $I_{a,k}$, and the discharging current of C_a ($I_{Ca,k}$) flow through rectifier diode D_1 and enter the DC side. Currents $I_{a,k}$ and $I_{Ca,k}$ flow through S_1, L_o, D_{o2} and return to the AC side. $I_{Lo,k} = I_{a,k} + I_{Ca,k}$. At the common point of the input capacitors (x), the returning current splits as $I_{a,k}$ and $I_{Ca,k}$. The voltage of the C_a at $t = t_1$, can be expressed as follows by considering its discharge:

$$V_{Ca,k(t1)} = V_{Ca,k(t0)} - \left(I_{Lo,k} - I_{a,k}\right)\left(t_1 - t_0\right) \Big/ C_a \qquad (3.1)$$

where $V_{Ca,k,(t0)}$ is the initial voltage or the peak value of v_{Ca} for the k^{th} switching cycle, and $I_{a,k}$ is the line current for phase A in k^{th} switching cycle. At the input side, $I_{a,k}$ further divides into $I_{b,k}$ and $I_{c,k}$ ($I_{a,k}$ = -$I_{b,k}$ - $I_{c,k}$). $I_{b,k}$ and $I_{c,k}$ respectively charge C_b and C_c. C_c begins to charge from $-V_2$ and reach voltage $V_{Cc,k(t1)}$ at $t = t_1$ when the mode ends, and its voltage can be expressed as follows:

$$V_{Cc,k(t1)} = -V_2 + {I_{a,k}(t_1 - t_0)}/{2C_c} \tag{3.2}$$

Mode 1 ends when C_a is fully discharged ($V_{Ca,k,(t1)}$ = 0); thus t_1 can be calculated as follows by rearranging Eq. (1):

$$t_1 = t_0 + {(C_a V_{Ca,k(t0)})}/{(I_{Lo,k} - I_{a,k})} \tag{3.3}$$

Mode 2 ($t_1 < t < t_2$), [Fig. 3.2(b)]:

At $t = t_1$, C_a becomes fully discharged and during this mode, C_a remains discharged, line current $I_{a,k}$ flows through D_1 and S_1, L_o and D_{o2}. $I_{a,k}$ returns to the input side and continues to charge C_b and C_c. $I_{Lo,k}$ freewheels through L_o, $D_{o1,}$ D_{o2} and the load.

Mode 3 ($t_2 < t < t_3$), [Fig. 3.2(c)]:

This mode begins at $t = t_2$ when S_1 is turned off. During this mode, both S_1 and S_2 are off and the AC input side is separated from the DC output side. In the AC input side, the phase currents continue to charge C_b and C_c, and C_a will begin to be charged by $I_{a,k}$. Mode 3 ends when S_2 is turned on at $t = t_3$ ($t_3 = t_0 + T_s/2$) due to the 180° phase shift between the two switches and the value of $V_{Ca,k}$ at the end of the mode is

$$V_{Ca,k(t3)} = {I_{a,k}(t_3 - t_2)}/{C_a} \tag{3.4}$$

Mode 4 ($t_3 < t < t_4$), [Fig. 3.2(d)]:

During Mode 4 C_a continues to be charged by $I_{a,k}$ while C_b and C_c are discharged by giving $I_{Cb,k}$ and $I_{Cc,k}$ respectively. The sum of the above currents flows through D_{o1}, L_o

and S_2. ($I_{b,k} + I_{Cb,k}$) and ($I_{c,k} + I_{Cc,k}$) return to the input side via D_6 and D_2 respectively. Mode 4 ends when C_b and C_c are discharged to a voltage level of $-V_2$ (these capacitors charge opposite to the reference directions shown in Fig. 4(b)) at $t = t_4$ as given below

$$t_4 = t_3 + \left\lfloor 2C_c\left(V_o + V_{Cc(t3)}\right)\right\rfloor / \left(I_{Lo,k} - I_{a,k}\right) \tag{3.5}$$

Mode 5 ($t_4 < t < t_5$), [Fig. 3.2(e)]:

During this mode, C_a continues to be charged by line current $I_{a,k}$ while the voltage across C_b and the voltage across C_c remain at $-V_2$. $I_{a,k}$ flows through D_{o1} while $I_{Lo,k}$

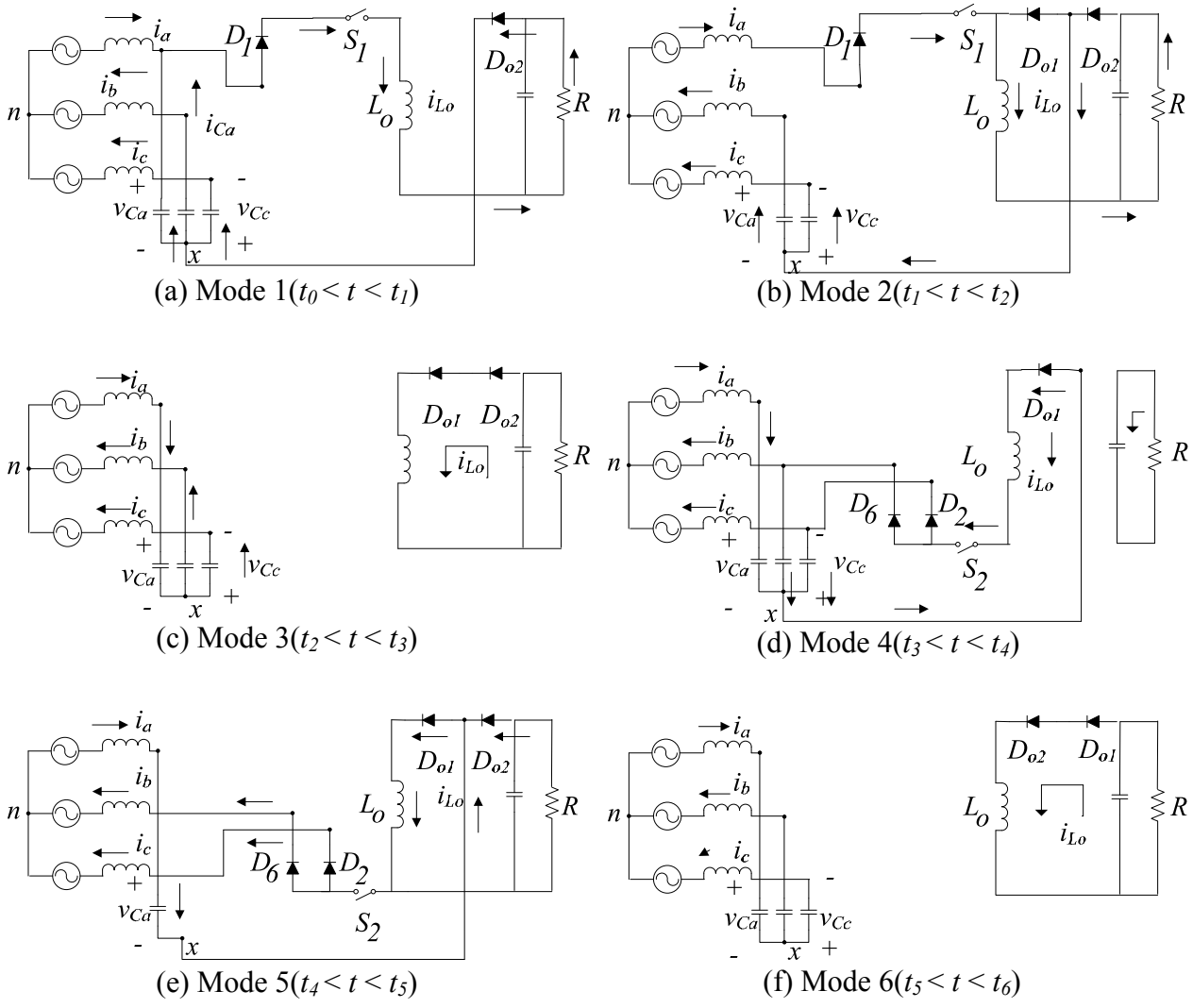


Fig 3.2: Modes of the converter when $D < 0.5$.

freewheels through L_o, D_{o2}, and the load.

Mode 6 ($t_5 < t < t_6$), [Fig. 3.2(f)]:

This mode begins when S_2 is turned off at $t = t_5$. Since both S_1 and S_2 are off, this mode is similar to Mode 3. During this mode, C_a reaches its peak voltage for k_{th} cycle while C_b and C_c begin to charge as given below

$$V_{Ca,k(t6)} = V_{Ca,k(t3)} + \left[I_{a,k}(T_s - t_3)\right] / C_a \tag{3.6}$$

$$V_{Cc,k(t6)} = -V_o + \left[I_{a,k}(1-D)T_s\right] / 2C_c \tag{3.7}$$

Mode 6 ends when S_1 is turned on at $t = t_6$ and the next switching cycle (k+1) begins.

3.2.2 D > 0.5 [Boost mode of operation]

It should be noted that unlike in the buck mode in the boost mode, the input capacitor discharging currents and the current of L_o are not constant during the k^{th} switching cycle; thus those variables are represented by lower-case letters below.

Before $t = t_0$, S_1 is off and S_2 is on. C_a is charged by line current $I_{a,k}$ while C_b and C_c discharge, giving currents $i_{Cc,k}$ and $i_{Cb,k}$ respectively.

Mode 1 ($t_0 < t < t_1$), [Fig. 3.4(a)]:

At $t = t_0$, S_1 is turned on and C_a begins to discharge; therefore $I_{a,k}$ and the discharging current of C_a ($i_{Ca,k}$) flow through switch S_1 and charge L_o, before returning to the AC side through switch S_2, D_6 and D_2. The discharging current of C_b is $i_{Cb,k}$. The current in D_6 equals $I_{b,k} + i_{Cb,k}$. The current in D_2 consists of $I_{c,k}$ and discharging current of C_c ($i_{Cc,k}$). Both diodes D_{o1} and D_{o2} are off. This mode ends when C_b and C_c are charged in the opposite direction to a voltage level that equals the output voltage ($-V_2$). The voltage of C_a at the end of Mode 1 is

$$V_{Ca,k(t1)} = V_{Ca,k(t0)} - \frac{1}{C_a}\int_{t_0}^{t_1}\left(i_{Lo,k} - I_{a,k}\right)dt \tag{3.8}$$

$V_{Ca,k(t0)}$ in Eq. (8) is the initial voltage of C_a and ($i_{Lo,k}$ - $I_{a,k}$) is C_a's discharging current.

$$V_{Cc,k(t1)} = V_{Cc,k(t0)} - \frac{1}{2C_c}\int_{t_0}^{t_1}\left(i_{Lo,k} - I_{a,k}\right)dt = -V_2 \tag{3.9}$$

The value of t_1 can be found by solving Eq. (3.9) above, which indicates the voltage of C_c at $t = t_1$. As explained above $V_{Cc,k(t1)}$ in Eq. (3.9) equals $-V_2$. Eq. 3.10 gives the current of L_o at $t = t_1$

$$I_{Lo,k(t1)} = I_{Lo,k(t0)} + \frac{1}{L_o}\int_{t_0}^{t_1}\left(v_{Ca,k} - v_{Cc,k}\right)dt \tag{3.10}$$

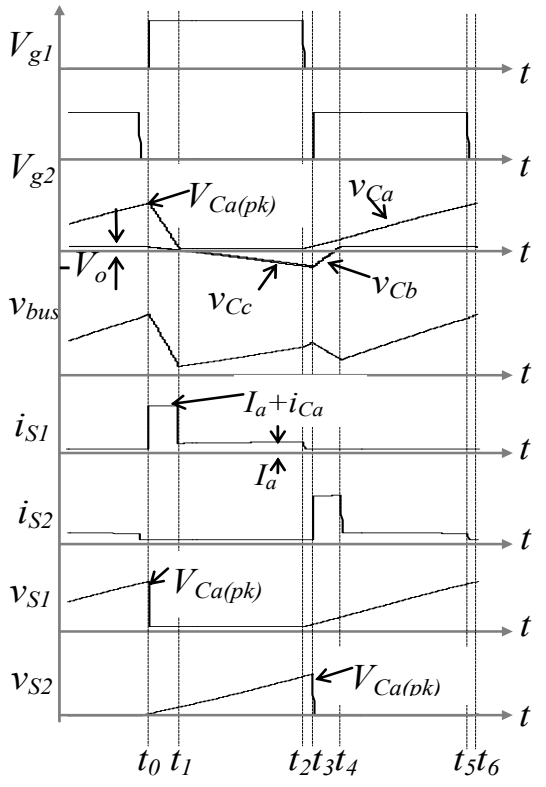


Fig 3.3: Typical waveforms when $D < 0.5$.

where the voltage across L_o is the DC bus voltage (v_{bus} in Fig. 3.8) and equals the line-to-line input capacitor voltage ($v_{Ca,k}$ - $v_{Cc,k}$).

Mode 2 ($t_1 < t < t_2$), [Fig. 3.4(b)]:

During Mode 2, C_a continues to discharge as in Mode 1 and $i_{Ca,k}$ flows through S_1, L_o and D_{o2}. Line current $I_{a,k}$ flows through D_1, S_1, L_o and S_2 before it divides into $I_{b,k}$ and $I_{c,k}$. Currents $I_{b,k}$ and $I_{c,k}$ flow through D_6 and D_2 respectively. The voltages across C_b and C_c remain at a voltage level of $-V_2$. The charging of L_o is given by Eq. (3.11)

$$I_{Lo,k(t2)} = I_{Lo,k(t1)} + \frac{1}{L_o}\int_{t_1}^{t_2}\left(v_{Ca,k} - V_2\right)dt \tag{3.11}$$

during Mode 2, the voltage across L_o is the difference between $v_{Ca,k}$ and V_2 because the voltage of C_c and C_b remain at $-V_2$.

Mode 3 ($t_2 < t < t_3$), [Fig. 3.4(c)]:

S_2 is turned off at the start of this mode. C_a continues to discharge and ($I_{a,k}$ + $i_{Ca,k}$) flows through L_o, R and D_{o2}, and returns to the input side. Currents $I_{b,k}$ and $I_{c,k}$ charge C_b and C_c, and charging of C_c can be explained as follow whereas the charging of C_b can be derived from Eq. (3.12):

$$V_{Cc,k(t3)} = -V_2 + \frac{I_{a,k}}{2C_c}\left(t_3 - t_2\right) \tag{3.12}$$

Eq. (3.13) can be used to find the current of L_o at $t = t_3$

$$I_{Lo,k(t3)} = I_{Lo,k(t2)} + \frac{1}{L_o}\int_{t_2}^{t_3}\left(v_{Ca,k} - v_{Cc,k}\right)dt \tag{3.13}$$

This mode ends when C_a is fully discharged and Eq. (3.8) is equated to zero to find $t = t_3$ as follows:

$$V_{Ca,k(t3)} = V_{Ca,k(t0)} - \frac{1}{C_a}\int_{t_0}^{t_3}\left(i_{Lo,k} - I_{a,k}\right)dt = 0 \tag{3.14}$$

Mode 4 ($t_3 < t < t_4$), [Fig. 3.4(d]:)

During Mode 4, C_a remains completely discharged. Throughout this mode, both output diodes D_{o1} and D_{o2} conduct current and the line current $I_{a,k}$ flows through D_1, S_1, L_o and D_{o2} and returns to the input side. $I_{b,k}$ charges C_b and $I_{c,k}$ charges C_c. The charging of C_c is given below by Eq. (15)

$$V_{Cc,k(t4)} = V_{Cc,k(t3)} + \frac{I_{a,k}}{2C_a}\left(t_4 - t_3\right) \tag{3.15}$$

where $t_4 = t_0 + T_s/2$ due to 180^o phase shift between the two switches. $i_{Lo,k}$ freewheels through D_{o1}, D_{o2} and R and has a final value of

$$I_{Lo,k(t4)} = I_{Lo,k(t3)} - \frac{V_2}{L_o}\left(t_4 - t_3\right) \tag{16}$$

Mode 5 ($t_4 < t < t_5$), [Fig. 3.4(e)]:

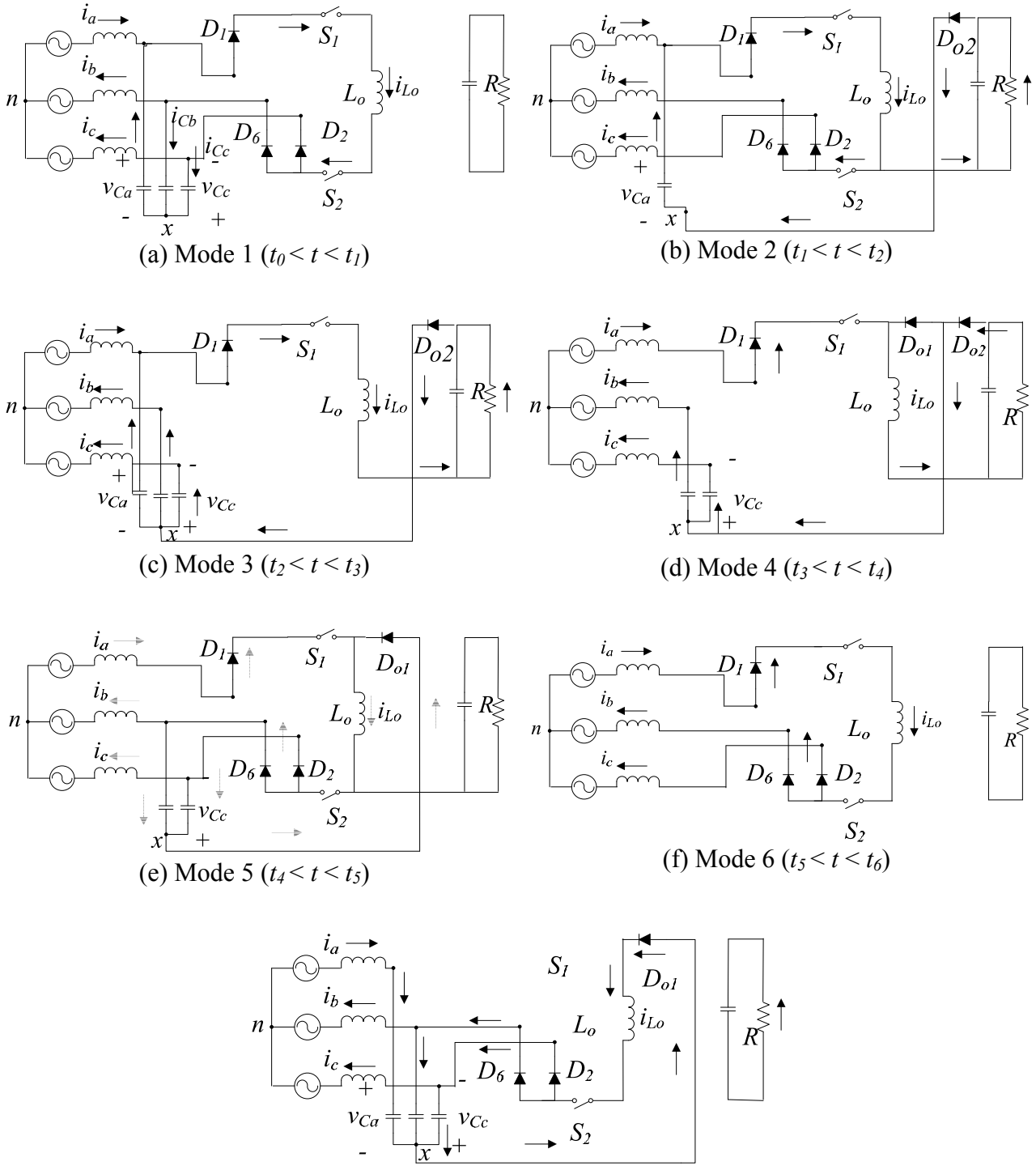
S_2 is turned on at $t = t_4$. Current $i_{Cb,k}$ flows out of C_b and $i_{Cc,k}$ flows out of C_c so that current (i_{Cb} + i_{Cc}) flows through D_{o1} and L_o. C_a remains discharged. The relevant equations for Mode 5 are as follows:

$$V_{Cc,k(t5)} = V_{Cc,k(t4)} - \frac{I_{a,k}}{2C_a}\int_{t_4}^{t_5}\left(i_{Lo,k} - I_{a,k}\right)dt \tag{3.17}$$

$$I_{Lo,k(t5)} = I_{Lo,k(t4)} + \frac{1}{L_o}\int_{t_4}^{t_5} v_{Cc,k}\,dt \tag{3.18}$$

Mode 6 ($t_5 < t < t_6$), [Fig. 3.4(f)]:

This mode begins when voltages of C_b and C_c are zero. All the input capacitors remain fully discharged as DC bus is short circuited. $I_{a,k} = -I_{b,k} - I_{c,k}$.



(a) Mode 1 ($t_0 < t < t_1$)

(b) Mode 2 ($t_1 < t < t_2$)

(c) Mode 3 ($t_2 < t < t_3$)

(d) Mode 4 ($t_3 < t < t_4$)

(e) Mode 5 ($t_4 < t < t_5$)

(f) Mode 6 ($t_5 < t < t_6$)

(g) Mode 7 ($t_6 < t < t_7$)

Fig 3.4: Modes of the converter when $D > 0.5$.

Mode 7 ($t_6 < t < t_7$), [Fig. 3.4(g)]:

At $t = t_6$, S_1 is turned off and $I_{a,k}$ starts to charge C_a. The difference in current between $i_{Lo,k}$ and $I_{a,k}$ is the total discharge of C_b and C_c. This mode ends at $t = t_7$ when S_1 is turned on. This is the start of the next switching cycle $k + 1$. Eq. (3.19) expresses the charging of C_a,

$$V_{Ca,k(t7)} = \frac{I_{a,k}}{C_a}(1-D)T_s \tag{3.19}$$

Eq. (3.20) expresses the discharging of C_c by considering the discharging current as $i_{Lo,k}$ - $I_{a,k}$

$$V_{Cc,k(t7)} = -\frac{1}{2C_a}\int_{t_6}^{t_7}(i_{Lo,k} - I_{a,k})dt \tag{3.20}$$

The current of L_o at the end of Mode 7 is

$$I_{Lo,k(t7)} = I_{Lo,k(t6)} + \frac{1}{L_o}\int_{t_6}^{t_7} v_{Cc,k}\,dt \tag{3.21}$$

The main difference between the proposed converter and the conventional three-phase AC-DC buck-boost converter [32] is that each of the switches in the proposed converter sees a line-to-neutral voltage (the voltage across one of the three input capacitors) across it rather than a line-to-line voltage (the voltage across two input capacitors), which is the case for the switch in the conventional converter. Since a switch in the proposed converter sees a line-to-neutral voltage instead of a line-to-line voltage, it has a peak voltage stress that is almost half that of the switch in the conventional converter as this stress is reduced by a factor of √3. The reduction of peak voltage stress allows lower rated devices to be used as converter switches and thereby extending the input voltage and/or load range the converter can operate.

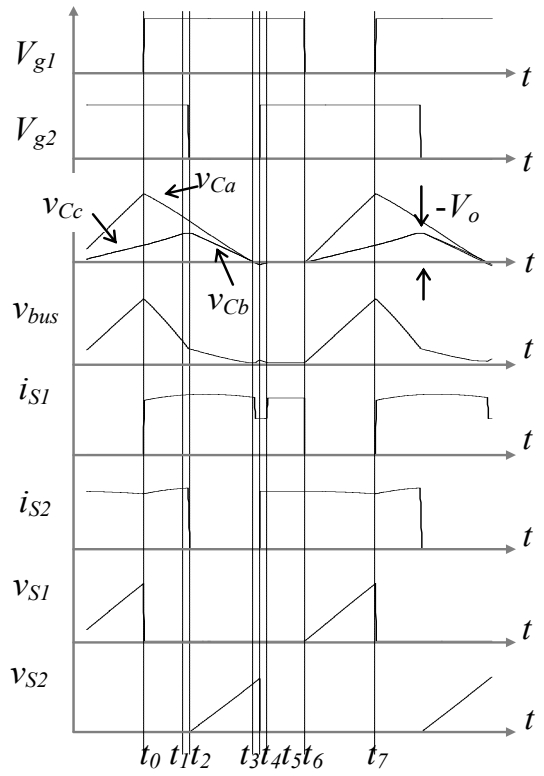


Fig 3.5: Typical waveforms when $D > 0.5$.

Another difference between the proposed converter and the conventional single-switch converter is that their input capacitor voltage waveforms are different. After the switch is turned on in the conventional converter, the input capacitors discharge and their voltages eventually falls to zero and remain zero until the switch is turned off. This is not the case for the proposed converter where the input capacitor voltages do not remain at zero, but, instead, continue to discharge (or charge in the opposite direction) until the voltage is $-V_2$. This is because of the connection between the mid-point of the output diodes and the common point of the input capacitors (x) in the proposed converter. This difference, as well as the difference in switch stresses, will be discussed in more detail later in the chapter.

3.3 Steady-State Analysis

In order to develop a procedure for the design of the converter, its steady-state characteristics must be determined first, by mathematical analysis. Once this has been done, graphs of characteristic curves can be generated and then used to develop a design procedure. In this section of the chapter, only the analysis for buck mode converter operation is presented in full detail because the input currents are more likely to be sinusoidal than when the converter is in boost mode operation and this simplifies the analysis.

When $D < 0.5$ (buck mode), the input capacitors' voltages are most likely to be discontinuous during all the switching cycles in a line cycle due to high circulating currents in the DC side of the AC-DC buck-boost converter. That is the input capacitors operate in DVM; hence the average input capacitor voltages are bounded by a sinusoidal envelope and as a result the input line currents are perfectly sinusoidal and the input power factor is excellent. The input capacitors, however, can be semi-continuous when $D > 0.5$ (boost mode), especially if the converter maximum power is low due to less current in the DC side. As a result, the input current will not be bounded by a sinusoidal envelope and the presence of harmonics will complicate the analysis.

Therefore, the best starting point for the mathematical analysis is to consider the buck operation of the converter under test, and then check whether the chosen operating point (input capacitors and input inductors) make the input capacitors operate in DVM or CVM and meet the IEC 61000-3-2 Class A harmonics standard. If the chosen operating point for buck mode satisfies the IEC standard in the boost mode, then the point is valid if not the procedure needs to be repeated and until the criteria is met to find a valid point.

3.3.1 Analysis for Buck mode of operation ($D < 0.5$)

The objective of the mathematical analysis is to find a relationship between the output-to-input voltage conversion ratio (M), input capacitor value (C), switching period (T_s) and the switch duty cycle (D) as they are the main parameters of the proposed converter. This relationship is found considering the energy balance of the converter; that is the total

input energy from all three-phases over a $\pi/6$ of the line cycle must be equal to the DC energy output to the load for the same duration provided the converter is lossless.

The procedure to determine output energy involves the multiplication of output DC voltage, output DC current and the time duration for $\pi/6$ of the line cycle. The procedure to determine the total input energy considers the sum of the energy in each phase, with the energy per phase dependent on the integration of the instantaneous energy (multiplication of instantaneous voltage and current) over a $\pi/6$ portion of the line cycle.

Based on assumption A_1 in Section 3.3, input phase voltage and current are considered as constants during a switching period so that they can be considered as DC parameters V_1 and I_1 for any particular switching cycle. As a result, an equivalent DC-DC buck-boost converter circuit with a LC filter can be used as a first step to find the instantaneous values that are required to find the desired relationship between M, input capacitor value (C), switching period (T_s) and the switch duty cycle (D).

The step-by-step process for the analysis of the converter operating in buck mode is as follows:

- **Step 1:** The analysis will begin by considering a DC-DC buck-boost converter with an LC filter shown in Fig. 3.6. An expression for the instantaneous input resistance will be determined in terms of input DC voltage (V_1), output voltage (V_2) (it should be noted that this output voltage is the same as the output voltage of the full three-phase converter), and D. The reason for finding the instantaneous input resistance (R_1) is because the instantaneous input current $I_1 = V_1/R_1$ and can be found using R_1 for any V_1 value for any switching cycle during the line cycle.

- **Step 2:** In this step, the DC source of the equivalent converter (which represents an instantaneous input voltage for any switching cycle during a line cycle) is replaced with a three-phase AC source. The single-phase LC filter is replaced by a three-phase LC filter and a diode bridge rectifier. Doing so results in a three-phase AC-DC single-switch version of the proposed converter. The expression for R_1 found in

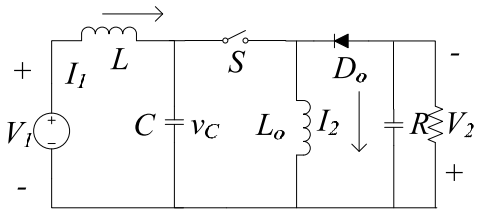


Fig 3.6: Dc-DC single-switch LC filter buck-boost converter.

Step 1 is used to find the instantaneous input line current for any switching cycle for any phase of the three-phase system for example $I_{a,k} = V_{a,k}/R_1$.

- **Step 3:** The input energy that is associated with each phase can be determined by multiplying the instantaneous input current determined in Step 2 with the input voltage and then integrating the result over an interval of $\pi/6$ of the line cycle [31]. The summation of the three-phase input energy gives the converter's the total input energy.

- **Step 4:** Assuming that the converter is ideal, the converter's total input energy can be equated with its output energy to determine the converter's output-to-input voltage conversion ratio for the buck mode of operation. This ratio is dependent on C_a, T_s and D. It should be noted that this ratio is for a single-switch version of the proposed converter that is derived by replacing the DC input source of the instantaneous single-switch DC-DC buck-boost converter used in Step 1 with a three-phase input. This ratio, however, is valid for the proposed converter, as will be explained in detail below after Step 4.

With this summary in mind, the analysis can proceed as follows:

A. Step 1: Calculating the instantaneous input resistance using DC-DC buck-boost converter

Fig. 3.6 shows the equivalent single switch buck-boost converter with a DC source. A single-phase LC filter is placed between the DC source (V_1) and the converter. The converter goes through three significant modes during steady-state operation and

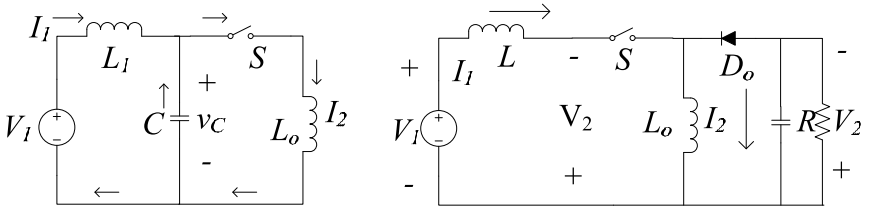
equivalent circuits for these modes and typical waveforms that are required for the analysis are given in Figs. 3.7 and 3.8 respectively. The three significant modes are as follows:

Mode 1 ($0 < t < t_1$), [Fig. 3.7(a)]: At $t = 0$, S is turned on and input capacitor C starts to discharge, giving a constant current I_2 - I_1, where I_2 is the output current and I_1 is the instantaneous input current. The diode D_o is off and the voltage of the diode is $v_D = V_C + V_2$. The switch current is I_2. During Mode 1, v_C becomes zero at $t = D_1T_s$ and continue to charge in the opposite direction to its reference direction shown in Fig. 3.6.

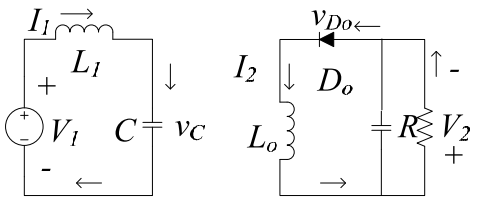
Mode 2 ($t_1 < t < t_2$), [Fig. 3.7(b)]: Mode 2 begins when $v_C = -V_2$; where V_2 is the output voltage but negative as the direction is opposite to the reference direction. During this mode, v_C remains at this voltage while the line current flows through S and L_o. D_o is forward biased and the current through it is I_2 - I_1.

Mode 3 ($t_2 < t < T_s$), [Fig. 3.7(c)]: At $t = DT_s$, S is turned off. C will start to be charged by I_1 and I_2 will flow through D_o. During this mode v_C crosses the time axis at $t = D_2T_s$ and continue to rise. At $t = T_s$, C reaches its peak voltage, V_{CM}.

The average voltage of input inductor L is zero at steady-state; therefore, when the



(a) Mode 1 ($0 < t < t_1$) (b) Mode 2 ($t_1 < t < t_2$)



(c) Mode 3 ($t_2 < t < t_3$)

Fig 3.7: Modes of operation of converter in Fig. 3.6 when $D < 0.5$.

loop that consists of V_1, L and C in Fig. 3.6 is considered, the average voltage of C must equal V_1, the instantaneous input voltage. The average voltage across C ($V_{C,ave}$) for a switching period can be found from its voltage waveform (v_C) shown in Fig. 3.8. When $V_{C,ave}$ is equated to V_1 then the following equation can be obtained:

$$V_{C,ave} = 0.5\left(\frac{V_{CM}D_1T_s + V_{CM}(1-D_3)T_s - V_2(D+D_3-D_2-D_1)T_s}{T_s}\right) = V_1 \qquad (3.22)$$

Eq. (3.22) consists of terms D_1, D_2 and D_3, where D_1 is the normalized time at which v_C becomes zero first (during discharging of C), D_2 is the normalized when v_C becomes $-V_2$ and D_3 is the normalized time when v_C becomes zero for the second time (during charging of C) as shown in Fig. 3.8.

Eqs. (3.23) and (3.24) can be used to reduce the variables D_2 and D_3 respectively from Eq. (3.22). Eqs. (3.23) and (3.24) are derived by considering the tangent of v_C curve shown in Fig. 3.10 and are as follows:

$$D_2 = D_1 + \frac{D_1V_2}{V_{CM}} \qquad (3.23)$$

$$D_3 = \frac{DV_{CM} + V_2}{V_{CM} + V_2} \qquad (3.24)$$

Substituting Eqs. (3.23) and (3.24) into Eq. (3.22) results in

$$\frac{D_1{V_{CM}}^2(V_{CM}+V_2) + {V_{CM}}^3(1-D) - V_2(V_{CM}+V_2)(DV_{CM} - D_1V_{CM} - D_1V_2)}{V_{CM}(V_CM + V_2)} = V_1 \qquad (3.25)$$

which gives the relationship between input voltage (V_1), duty ratio (D), the normalized time point at which v_C crosses zero axis (D_1) and the peak capacitor voltage (V_{CM}).

In order to find the instantaneous resistance R_1 after obtaining Eq. (3.25), input current I_1 must be found next. I_1 can be calculated by considering the charging of C from minimum voltage V_2 to its peak voltage V_{CM} in Mode 3 (Fig. 3.7(c)). During Mode 3, the

entire source current I_1 is used to charge C for the duration of $dt = (1 - D)T_s$ until S is turned on again; this can be expressed by

$$I_1 = C\frac{dv_C}{dt} \tag{3.26}$$

or by Eq. (3.27) where $dv_C = V_{CM}+V_2$, according to Fig. 3.8,

$$I_1 = C\left(\frac{V_{CM} + V_2}{(1-D)T_s}\right) \tag{3.27}$$

R_1 can now be calculated by dividing Eq. (3.25) by Eq. (3.27) and can be expressed as

$$R_1 = \frac{(1-D)D_1^2 T_s}{2CD^2} \tag{3.28}$$

In order to further reduce variables from Eq. (3.28), D_1 needs to be removed; thus the steady-state operation of the loop L_2, D_o and V_2 of Fig. 3.6 was considered. The average voltage across output inductor L_2 is also zero at steady-state; as a result, the average voltage across diode D_o ($V_{Do,ave}$) should equal V_2, the output DC voltage. The instantaneous voltage of D_o (v_{Do}) has a triangle shape according to Fig. 3.8. $v_{Do} = v_C + V_2$. At $t = 0$, v_{Do} starts from peak voltage and becomes zero at $t = D_2T_s$; therefore, $V_{Do,ave}$ can be expressed as

$$V_{Do,ave} = \frac{(V_2 + V_{CM})D_2T_s}{2T_s} = V_2 \tag{3.29}$$

When D_2 is removed from Eq. (3.29) using Eq. (3.23), the result is

$$\frac{(V_2 + V_{CM})(D_1V_{CM} + DV_2)}{2V_{CM}} = V_2 \tag{3.30}$$

Eq. (3.30) can be rearranged to find D_1 in order to remove it from Eq. (3.28) to reduce the number of variables in the R_1 expression to obtain Eq. (3.32) below

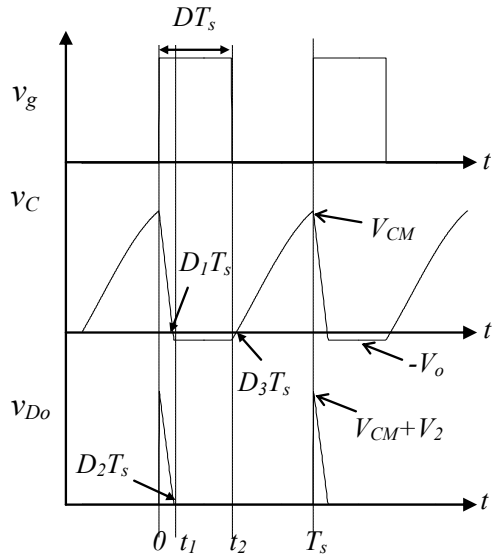


Fig 3.8: Typical waveforms for DC-DC buck-boost converter when $D < 0.5$.

$$D_1 = \frac{2V_2}{V_{CM} + V_2} - \frac{DV_2}{V_{CM}} \tag{3.31}$$

$$R_1 = \frac{T_s}{2C}(1-D)\left(1-D+\frac{2V_2}{V_{CM}}\right) \tag{3.32}$$

B. Step 2 : Calculation of the instantaneous line currents for a three-phase single-switch buck-boost converter

This step of the analysis uses the input resistance equation to find the input currents during each switching cycle for the three-phase system (Fig. 3.9). The instantaneous input voltages for a balanced three-phase system are

$$v_a(\omega_l t) = V_1 \sin(\omega_l t) \tag{3.33}$$

$$v_b(\omega_l t) = V_1 \sin\left(\omega_l t - 2\pi/3\right) \tag{3.34}$$

$$v_c(\omega_l t) = V_1 \sin\left(\omega_l t - 4\pi/3\right) \tag{3.35}$$

where V_1 is peak phase voltage and ω_l is the angular line frequency. The instantaneous input line currents can be obtained by the ratio of input voltage to the input resistance corresponding to each phase. For example, the current in phase A is

$$i_a(\omega_l t) = \frac{v_a(\omega_l t)}{R_1} = \frac{2CV_{CM}V_1 \sin(\omega_l t)}{T_s(1-D)\left[V_{CM}(1-D)+2V_2\right]} \tag{3.36}$$

Currents for phases B and C are analogous to Eq. (3.36) but phase shifted by 2π/3.

C. Step 3 : Calculation of the three-phase input energy

This step of the analysis is to calculate the total input energy for the three-phase system by summing the integrals of the instantaneous energy over π/6 of the line cycle for each of the three phases. The input energy of phase A for $\pi/3 \le \omega_l \le \pi/2$ can be derived as follows:

$$W_a = \int_{\pi/3}^{\pi/2} v_a(\omega_l t) i_a(\omega_l t) d(\omega_l t) \tag{3.37}$$

where $v_a(\omega_l t)$ and $i_a(\omega_l t)$ are the instantaneous phase A voltage and current obtained in Step 2, by substituting the values from Eqs. (3.33) and (3.36) in Eq. (3.37) gives

$$W_a = \int_{\pi/3}^{\pi/2} \frac{2CV_{CM}}{T_s(1-D)\left[V_{CM}(1-D)+2V_2\right]} \left(V_1 \sin(\omega_l t)\right)^2 d(\omega_l t) \tag{3.38}$$

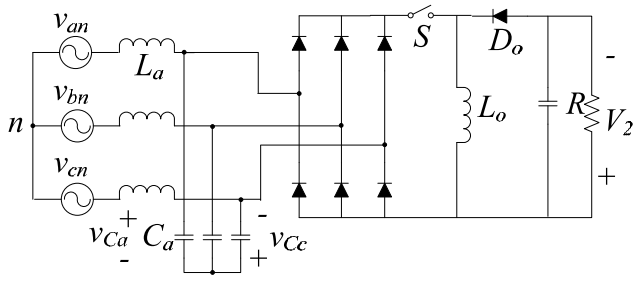


Fig 3.9: Three-phase AC-DC single-switch buck-boost converter.

$$W_a = \frac{V_1^2 C V_{CM}}{T_s(1-D)\left[V_{CM}(1-D)+2V_2\right]} \int_{\pi/3}^{\pi/2} \left(1-\cos(2\omega_l t)\right) d(\omega_l t) \tag{3.39}$$

and solving Eq. (3.39) yields

$$W_a = \frac{V_1^2 C V_{CM}}{T_s(1-D)\left[V_{CM}(1-D)+2V_2\right]} \left(\frac{\pi}{6} + \frac{\sqrt{3}}{4}\right) \tag{3.40}$$

Similarly, the input energy for phases B and C can be given also be obtained by replacing the voltage and current in Eq. (3.37) by the relevant values

$$W_b = \frac{V_1^2 C V_{CM}}{T_s(1-D)\left[V_{CM}(1-D)+2V_2\right]} \left(\frac{\pi}{6} - \frac{\sqrt{3}}{2}\right) \tag{3.41}$$

$$W_c = \frac{V_1^2 C V_{CM}}{T_s(1-D)\left[V_{CM}(1-D)+2V_2\right]} \left(\frac{\pi}{6} + \frac{\sqrt{3}}{4}\right) \tag{3.42}$$

The total input energy W_i is

$$W_i = W_a + W_b + W_c \tag{3.43}$$

which results in

$$W_i = \frac{V_1^2 C V_{CM}}{T_s(1-D)\left[V_{CM}(1-D)+2V_2\right]} \left(\frac{\pi}{2}\right) \tag{3.44}$$

D. Step 4 : Derivation of the mathematical relationship between M, C T_s and D

For the energy equilibrium of the converter, the output energy (W_o) must be equal to the input energy (W_i). $W_o = W_i$. W_o over the interval of π/6 of fundamental period can be expressed as

$$W_o = \frac{\pi}{6} \frac{V_2^2}{R} \tag{3.45}$$

where V_2 is the output DC voltage and R is the load resistance. Substituting for W_o and W_i using Eqs. (3.45) and (3.44), and rearranging the results leads to the following relationship:

$$\frac{V_2^2}{3V_1^2} = \frac{CRV_{CM}}{T_s(1-D)\left[V_{CM}(1-D)+2V_2\right]} \tag{3.46}$$

If the output-to-input voltage conversion ratio (M) is defined as the ratio of output voltage (V_2) to line-line peak input voltage, then M can be expressed as a function of C, T_s, and D as follows:

$$M = \frac{V_2}{\sqrt{3}V_1} = \sqrt{\frac{CRV_{CM}}{T_s(1-D)\left[V_{CM}(1-D)+2V_2\right]}} \tag{3.47}$$

Eq. (3.47) gives M as a function of C and D for a three-phase AC-DC single-switch version of the proposed buck-boost converter and was derived by considering the input capacitor voltage waveform and the energy equilibrium of this single-switch converter. Although Eq. (3.47) was derived for the single-switch version of the proposed converter, it is valid for the proposed converter because the input capacitor voltages have comparable shapes and the peak input capacitor voltages for any switching cycle are the same.

Typical input capacitor voltage waveforms for the single-switch converter and the proposed two-switch converter are given in Fig. 3.10. The main difference in the two sets of waveforms is the timing when the input capacitor voltages rise and fall. As can be seen in Fig. 3.10(a), all three capacitors charge when the switch is off and they discharge when the switch is on in the single-switch converter. On the other hand, as can be seen in Fig. 3.10(b), C_a charges when S_1 is off and discharges when S_1 is on while C_b and C_c charge when S_2 is off and discharge when S_2 is on in the proposed two-switch converter. In other words, for any given switching cycle, the rise and fall of the input capacitor voltages are dependent on the turning on and turning off of the single switch in the single-switch converter, but in the proposed converter, the rise and fall of some capacitor voltages are associated to switch S_1 while the rise and fall of the other capacitor voltages others are

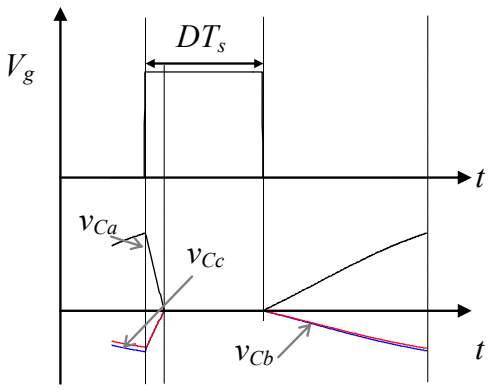
linked to S_2. Unlike in Fig. 3.10(a), not all input capacitors charge and discharge at the same time in Fig. 3.10(b) because S_1 and S_2 operate with 180° phase shift. Since both converters can operate with the same D for the same instantaneous input voltage value, the shape of the input voltage waveforms will be the same; therefore, Eq. (3.47) is still valid for the proposed converter and can be used to find the duty cycle and input capacitance of the proposed two-switch buck-boost converter.

Graphs of curves of M vs. D for different input capacitors when the converter operates in the buck mode can be plotted based on Eq. (3.47) using MATLAB. Such graphs can be used as part of a design procedure as shown in Section 3.6.

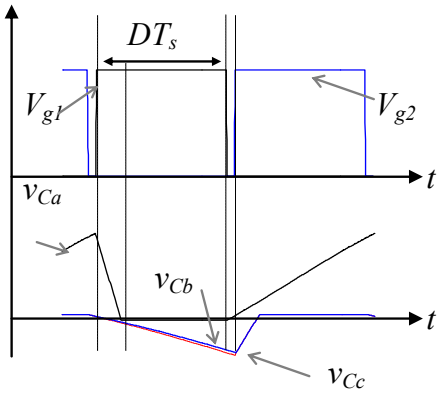
3.3.2 Analysis for Boost mode of operation (D > 0.5)

The analysis for boost mode operation differs from that of buck mode operation because the input capacitor voltages (and thus the input currents) are less likely to be sinusoidal and more likely to be distorted. The fact that the input currents are probably not sinusoidal complicates the analysis of boost mode operation and thus an approach that is different from the one used for buck mode analysis is needed.

The operation of the converter when it is in boost mode and its input capacitor



(a). Three-phase AC-DC single-switch buck-boost converter



(b). Three-phase AC-DC two-switch buck-boost converter

Fig 3.10: Typical input capacitor voltages for a switching cycle when D < 0.5.

voltages are operating in continuous voltage mode (CVM) is summarized as follows: At $t = t_0$, S_1 is turned on and C_a begins to discharge while C_b and C_c continue to discharge. $I_{a,k}$ and $i_{Ca,k}$ flows through S_1, L_o and S_2. D_{o1} and D_{o2} are off. This is same as Mode 1 shown in Fig. 3.5(a); thus modal Eqs. (3.8) - (3.10) define this mode. At $t = t_1$, the voltages across C_b and C_c equal $-V_2$ and only C_a discharges during this mode. $i_{Ca,k}$ flows through D_{o1}, and D_{o2} is still off. This is same as Mode 2 shown in Fig. 3.5(b); thus modal Eqs. (3.8) and (3.11) can be used to find the necessary variables. Mode 3 begins when S_2 is turned off at $t = t_2$, C_b and C_c begin to charge by $I_{b,k}$ and $I_{c,k}$ respectively while C_a continues to discharge. The first main difference between DVM and CVM is that, at the end of this mode C_a is not fully discontinuous as in Mode 3 of Fig. 3.5(c); instead, Mode 3 for CVM ends when S_2 is turned on at $t = t_3$. Modal Eqs. (3.12) - (3.14) can be used to find mode end variable values. Mode 4 for CVM is the same as Mode 1 described above where both S_1 and S_2 are on and all the capacitors discharge; therefore Eqs. (3.8) - (3.10) can be used to define Mode 4 but with new initial conditions. At $t = t_4$, S_1 is turned off and C_a begins to charge using $I_{a,k}$. Total discharge of C_b and C_c flows through D_{o2} and this mode is same as Mode 7 shown in Fig. 3.5(g); thus modal Eqs. (3.19) - (3.21) can be used to define the mode. At the end of this mode S_1 is turned on again and a new switching cycle begins.

Given the interdependency of the components and key variables such as input capacitor voltage $v_{Ca,k}$, output inductor voltage $v_{Lo,k}$, etc. the analysis of the converter in the boost mode cannot be performed using equations with closed form solutions and some sort of a computer program must be used to solve the aforementioned modal equations.

The objective of the boost mode analysis is to confirm that a chosen value of C_a obtained from an analysis of the buck mode is satisfactory for boost mode operation as well. In order to do this, it must first be determined that the converter is operating at steady-state for the chosen value of C_a and a randomly selected D. If it is determined that the selected D does not result in converter steady-state operation, then it must be changed until it does so. Once it has been determined that the converter is in steady-state operation, instantaneous input capacitor voltage waveforms can be determined for a line

cycle and used to determine the input current waveforms to see if they meet the appropriate harmonic standard, without undue stress placed on the converter components. If these criteria are not met, then a different value of C_a must be selected.

As a result of the above-mentioned considerations, especially the fact that the converter input currents for boost mode operation are likely to be distorted (and not sinusoidal as in buck mode operation), some sort of computer program is needed for the boost mode analysis. One way to develop this computer program is to consider the following: First, as a starting point, a random value of D (slightly above 0.5) for boost operation is selected and the value of C_a used is the value that was already chosen to give the required output voltage and that ensures DVM operation of C_a in the buck mode. If the converter is in steady-state for the chosen operating point in boost mode, the average voltage across an inductor or average current through a capacitor must be zero. For this analysis, the status of the converter can be checked by calculating the average value of the L_o voltage, $V_{Lo(ave)}$, over a line cycle. To do this, the instantaneous L_o voltage must be divided by T_l. If $V_{Lo(ave)} = 0$, for this period, then the converter is in steady-state and a steady-state operating point has been determined (D is valid). If not, the value of D should be incremented until the steady-state criterion is satisfied. Then, based on $v_{Ca,k}$ and the sinusoidal input phase A voltage, the voltage across an input inductor L_a can be found ($v_{La,k}$). Based on $v_{La,k}$ the instantaneous current of L_a, $i_{La,k}$ can be obtained and the Fast Fourier Transform [FFT($i_{La,k}$)] can be performed to check if the IEC standard is met. If not a much smaller C_a for buck mode must be selected and its suitability for boost mode should be rechecked.

To find the instantaneous voltages for the k^{th} switching cycle such as $v_{Ca,k}$, $v_{Lo,k}$, etc. , the process should start with some initial values ($V_{Ca,k(t0)}$, $I_{a,k}$) for Mode 1; then based on modal Eqs. (3.8) - (3.9), the variable values at the end of Mode 1 (e.g. $V_{Ca,k(t1)}$) can be calculated, taking these values as the initial conditions for Mode 2; the values at $t = t_2$ can be found using the modal equations that define Mode 2. This way the variable values for all the modes in the k^{th} switching cycle can be obtained. After the program checks whether one whole switching cycle is calculated ($t_7 = t_0 + T_s$) the values of the next switching cycle can be derived based on the final variable values for k^{th} switching cycle

(i.e. $V_{Ca,k(t7)} = V_{Ca,k+1(t0)}$). This process will repeat until all the switching cycles for one line cycle are obtained by iterating $k = T_l/T_s$ times (where T_l is the line period and T_s is the switching period). After this has been done, the program can proceed to check if the converter is operating in steady-state or not. If the answer is "no", then D should be increased and the process described above must be repeated; if the answer is "yes", then the FFT can be obtained as explained above to check to see if the IEC standard is met.

A flowchart of the computer program described in this section is shown in Fig. 3.11.

3.4 Design and Example

In this section of the chapter, a procedure that can be used to determine the key parameters of the proposed converter (the input capacitors, inductors and the duty ratio) is presented and demonstrated with an example. The output filter components can be determined in the same manner as those of a conventional buck-boost converter [18] and a procedure for their design is not given here. For the example, the converter specifications will be an input line-line rms voltage V_{in} = 220 V, an output voltage V_2 = 150 V (D < 0.5) and 500 V (D > 0.5), a maximum output power $P_{o,max}$ = 2 kW and a switching frequency f_s = 25 kHz.

A. Selecting the Input Capacitors ($C_a = C_b = C_c$)

In order to select an input capacitor value (C_a), either the buck or the boost mode of operation should be considered first and converter operation should be confirmed for the other mode. C_a is more likely to be fully discontinuous throughout the input line cycle when the converter is in buck mode as mentioned in Section 3.4. Therefore, based on Eq. (3.47) derived by mathematical analysis, a suitable C_a for the required output-to-input voltage conversion ratio (M) and duty ratio (D) for buck mode operation can be selected using appropriate design curves shown in Fig. 3.12.

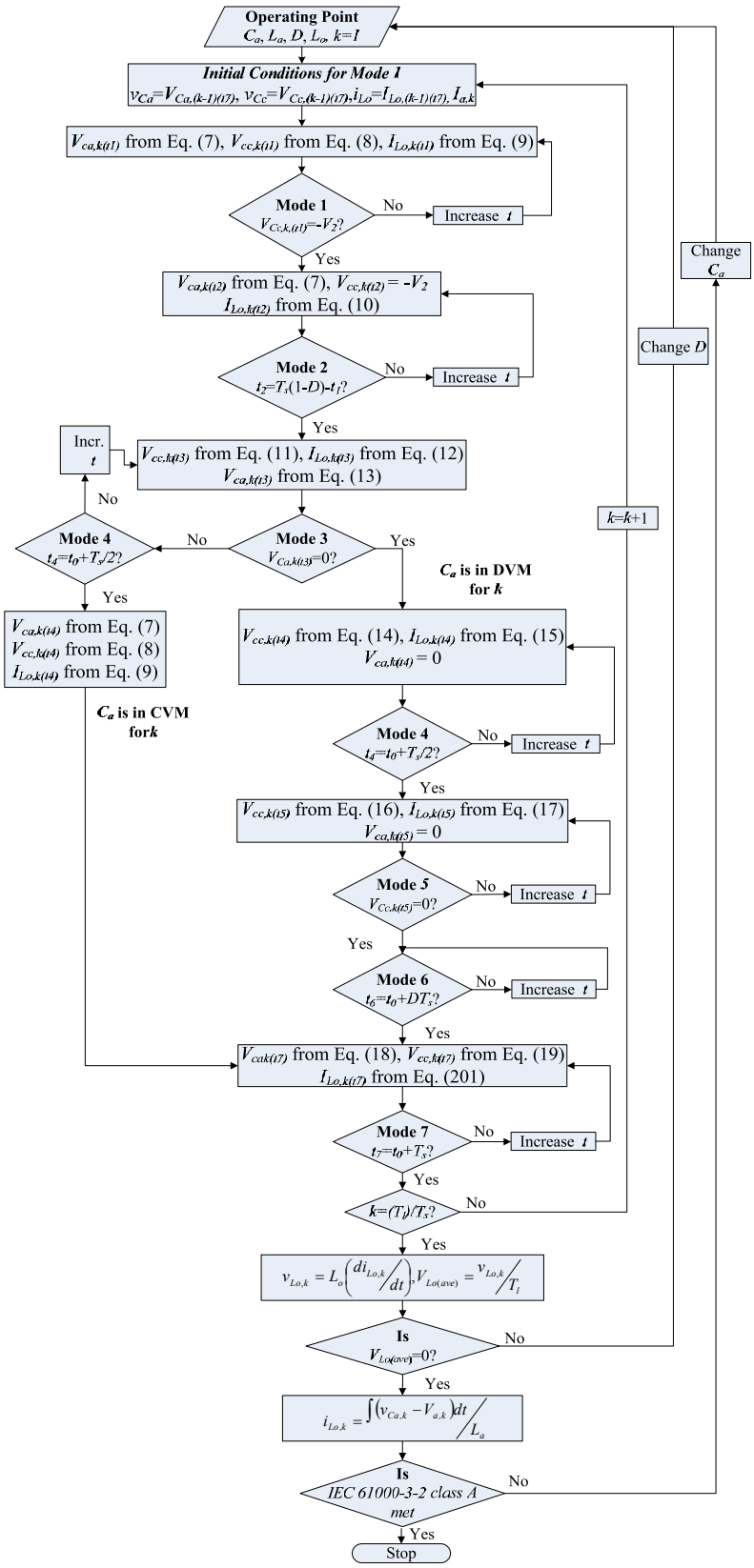


Fig 3.11: Flowchart of mathematical analysis.

Although a particular value of C_a may be satisfactory for buck mode converter operation, it may be unsuitable for the converter operating in boost mode because that input current harmonics standard may not be satisfied as the voltage across C_a may not be fully discontinuous throughout the line cycle. Some sort of compromise therefore must be considered as increasing the value of C_a to reduce switch stresses in the buck mode may result in a too large C_a in the boost mode to ensure an input current that is compliant with IEC standard. As a result of this compromise it is necessary to confirm that the converter designed for buck mode can meet the IEC standard when it is operated in the boost mode, the design procedure is therefore iterative. In this section, only the final iteration of the design example is shown.

Based on the converter specifications, M can be calculated ($M = V_2/\sqrt{3}V_1$). If D is closer to 0.5, then C_a that will be in DVM for all the switching cycles can be obtained using the characteristic curves shown in Fig. 3.13, which shows a set of curves of M vs. D for a range of C_a values. $M < 1$ and $0 \leq D \leq 0.5$ for buck operation. Each curve with markers refers to a different C_a value [20 nF < C_a < 250 nF]. The solid straight line which goes through the origin indicates M vs. D during the boundary discontinuous voltage mode (BDVM). That is if the operating point lies on the straight-line without markers, then when $D < 0.5$ C_a's voltage will touch zero axis exactly when $t = DT_s$, in the critical switching cycle where phase voltage is at its peak. Therefore, any operating point that is in the area below the straight line will ensure DVM operation of C_a.

The higher the value of C_a, the lower will be the peak switch voltage ($V_{s,pk}$) so that it is important to select the highest capacitance that will ensure the DVM operation of C_a. According to Fig. 3.13, when C_a = 220 nF and the D is approximately 0.5, the proposed converter operates in DVM; therefore, for this iteration, C_a was chosen as 220 nF. Once C_a for $D < 0.5$ is selected the next step is to perform the "check" in order to find out if the converter meets the IEC standard in the boost mode or not.

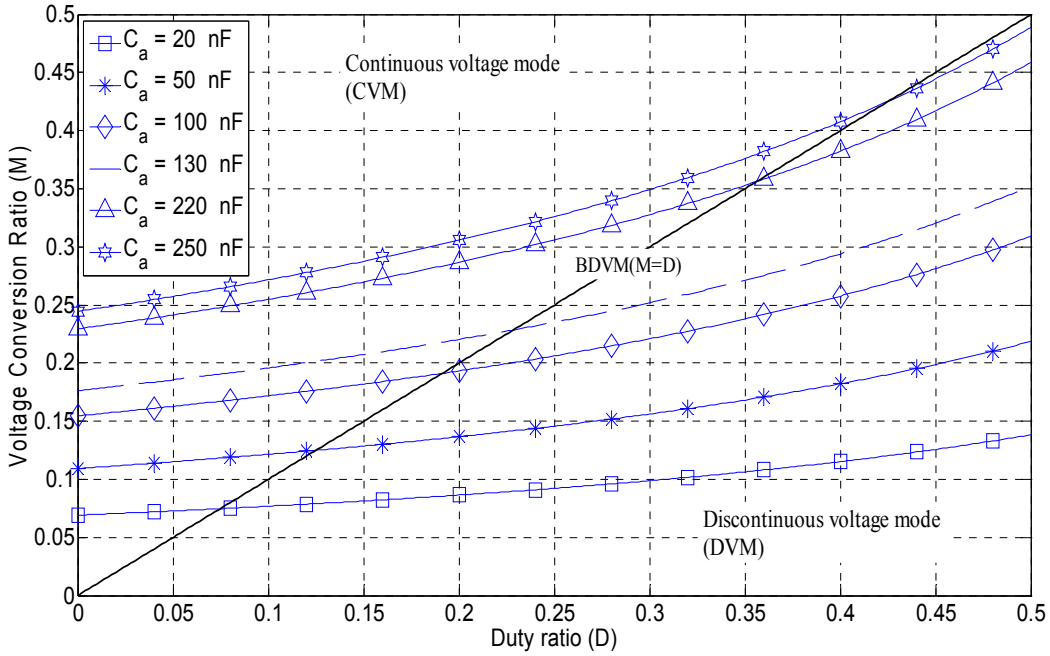


Fig 3.12: Voltage conversion ratio (M) vs. duty ratio (D) for the proposed converter when $D < 0.5$.

B. Selecting the Input Inductor ($L_a = L_b = L_c$)

The design of the converter in the previous steps is based on the assumption that the input currents are perfectly sinusoidal. In reality, this is not true as these currents will have high–frequency ripple and low–frequency harmonics. When $D < 0.5$ there is more current available to discharge the input capacitors. This makes it more likely that the input capacitor voltages will be fully discontinuous and thus more likely that the input currents will be sinusoidal. As a result, it is the high–frequency ripple that is more dominant when the converter is operating $D < 0.5$.

Fig. 3.13 shows a per phase equivalent circuit of L–C filter section that can be used to find the relationship between C_a, L_a and the line current harmonics. If f_r is the dominant harmonic frequency (sidebands) related to the switching frequency f_s then f_r can be written as Eq. (3.47), gives the allowed high frequency input ripple current in to the utility side (I_{lfr}) as a function of total generated harmonics (I_{tfr}) and input parameters

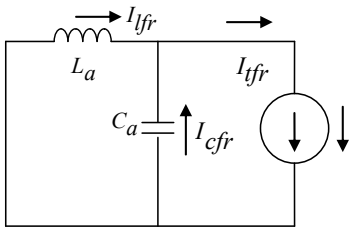


Fig 3.13: Single-phase equivalent L-C filter circuit.

$$I_{lfr} = I_{tfr}\left(\frac{1/2\pi f_r C_a}{2\pi f_r L_a - 1/2\pi f_r C_a}\right) \tag{3.48}$$

If $I_{lfr} = 20\% I_{tfr}$, then the relationship between the input filter components and harmonic content becomes

$$L_a C_a = \left(1/2\pi f_r\right)^2 \left(1 + I_{tfr}/0.2 I_{tfr}\right) \tag{3.49}$$

where C_a = 220 nF and f_r = 25060 Hz or 24940 Hz. L_a becomes 1.1 mH.

C. Selecting the Duty Ratio D and Checking IEC Standard Compliance in the Boost Mode

With value of C_a chosen above and the D that allows the converter boost operation to reach the steady-state; the next step of the design procedure is to confirm that the input current harmonic standard is satisfied for boost operation. This done by finding the FFT of the input inductor current $i_{La,k}$ as shown as the last step of the flowchart in Fig. 3.11. For this example, such a check was performed and the harmonic content was found to be satisfactory with respect to IEC 61000-3-2 Class A. If this had not been the case, then a new C_a needed to have been found.

D. Peak Switch Voltage

The converter can encounter the peak switch voltage when it is operating in the buck mode or in the boost mode. As a result, the peak switch voltage must be checked for both modes of operation, as shown in this section, to determine the actual peak switch voltage.

For buck operation

The peak switch voltage in the buck mode of operation occurs when the converter is at the full load and at the switching cycle where the phase voltage is at its peak. Due to the placement of the switches, $V_{s(pk)}$ is limited to the maximum phase voltage of the C_a so that the switch stress is about half of the peak switch voltage stress of a switch in the conventional single-switch three-phase buck-boost converter (Fig. 3.2). This switch stress can be found as

$$V_{s,pk} = \frac{I_{a,pk}}{C_a}(1-D)T_s \tag{3.50}$$

In Eq. (3.50), $I_{a(pk)}$ = 7.5 A(= ($\sqrt{2}\ P_{o,max}$)/($\sqrt{3}V_{in}$)), the selected C_a = 220 nF and D = 0.5 (which was determined from Fig. 3.11), and the switching period T_s = 40 μs. The resultant switch voltage stress at this operating point is approximately 700 V.

For boost operation

For the selected operating point, v_{Ca} is semi-continuous for boost mode. This was found by the instantaneous input capacitor voltage (v_{Ca}) found by the flowchart shown in Fig. 3.11. As a result the maximum switch stress can occur during any switching cycle and this value will be dependent on the minimum value of $v_{Ca,k}$ or the voltage value when switch is turned off and the line current $I_{a,k}$ for that switching cycle. To find these values in order to calculate $V_{s(pk)}$ a sweep must be performed using the flowchart in Fig. 3.11.

$$V_{s(pk)} = V_{Ca,k(t4)} + I_{a,k}(1-D)T_s / C_a \tag{3.51}$$

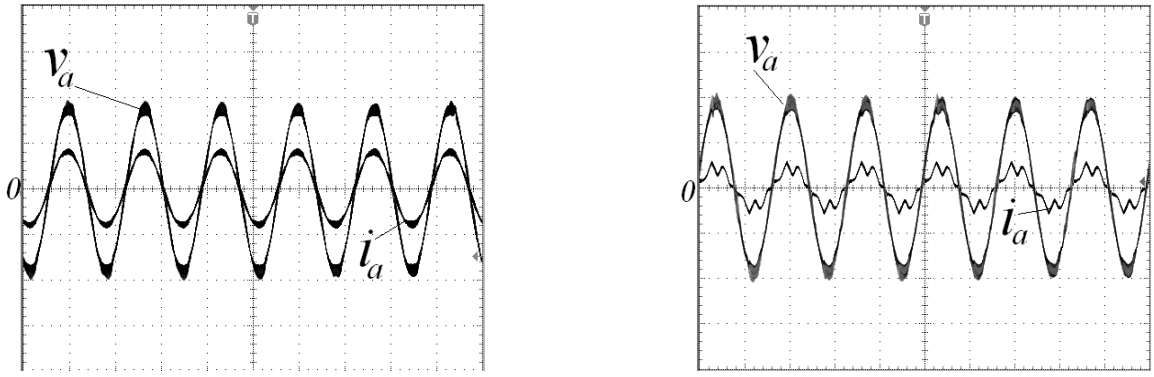
the values obtained from the sweep were $I_{a,k}$ = 6A and $V_{Ca,k(t4)}$ = 450V, and they resulted in a $V_{s,pk}$ of approximately 800 V.

3.5 Experimental Results

A simple, proof-of-concept, experimental prototype of the proposed converter was built to confirm its feasibility. The converter was implemented with main circuit components $L_a = L_b = L_c$ = 1.3 mH, $C_a = C_b = C_c$= 220 nF, L_o = 1.3 mH and C_o = 1500 μF at switching frequency f_s = 25 kHz. The experimental waveforms were obtained when the converter operates with input voltage V_{in} = 220 V, output voltages V_2 = 150 V (D < 0.5) and 500 V (D > 0.5), and maximum output power $P_{o,max}$ = 2 kW. The semiconductors used for the prototype are FGA50N100BNTD2 as switches and APT30DQ100BG-ND as rectifiers.

Figs. 3.14 – 3.20 show the following experimental results:

- Fig. 3.14 shows typical input current waveforms when V_2 = 150 V (Fig. 3.14(a)) and 500 V (Fig. 3.14(b)) and P_o = 2 kW. It can be seen from Fig. 3.14 that the input current waveform when V_2 = 150 V has considerably less distortion than that when V_2 = 500 V. This is because there is more current available to discharge the input capacitors at the lower output voltage than at the higher input voltage.

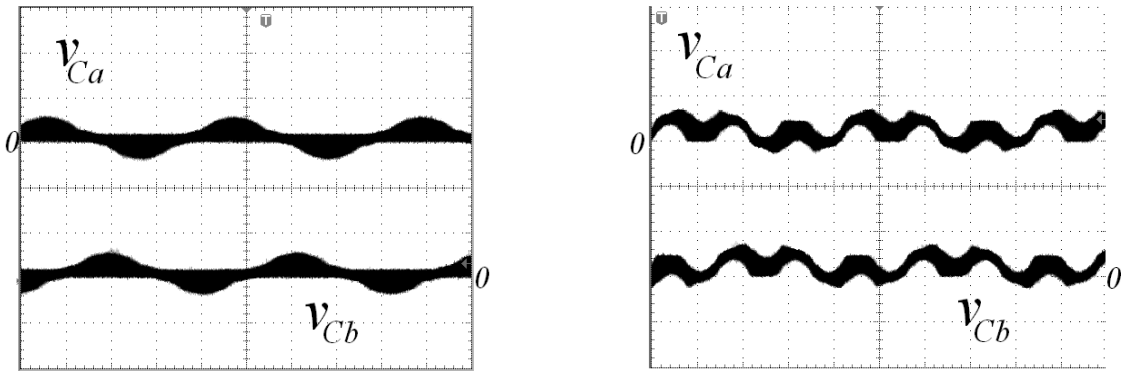


(a). V_2 = 150 V (b). V_2 = 500 V

Fig 3.14: Phase voltage and line current $P_{o,max}$ = 2 kW [V: 100 V/div, I: 10 A/div, t: 10 ms/div].

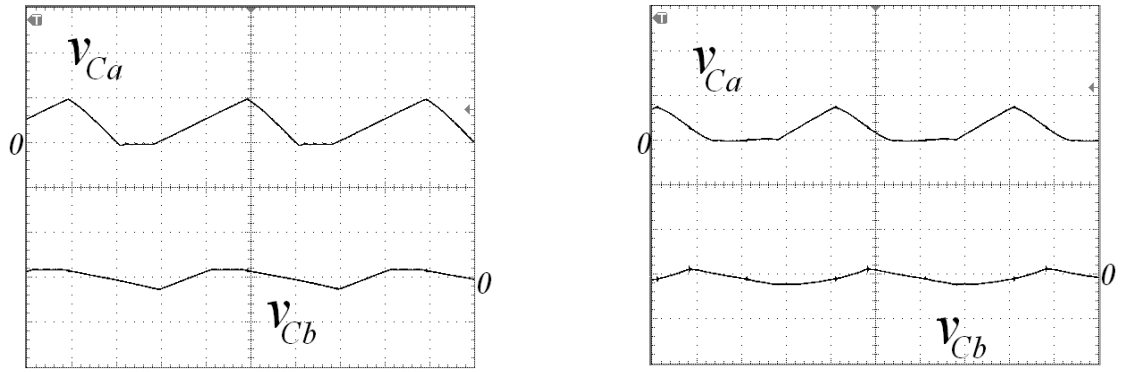
- Fig. 3.15 shows typical input capacitor voltage waveforms (v_{Ca}, v_{Cb} and v_{Cc}) when V_2 = 150 V [Fig. 3.15(a)[and 500 V [Fig. 3.15(b)] and P_o = 2 kW. It can be seen in Fig. 3.15(a) that the input capacitor voltages are in the DVM and bounded by a sinusoidal envelope so that they themselves can be considered to be sinusoidal whereas the waveforms in Fig. 3.15(b) are semi-continuous waveforms and do seem to be sinusoidal at all.

- Figs. 3.17 and 3.18 show input voltage (v_a) and current (i_a) waveforms for V_2 = 150 V and 500V, for various loads. Tables 3.1 and 3.2 show the input line current harmonics for various loads when V_2 = 150 V and 500 V respectively. It can be seen from Figs. 3.17 and 3.18 that the input current waveforms becomes less distorted as the load is increased and that the waveforms for V_2 = 150 V are less distorted than those for V_2 = 500 V. This is because more load current results in the input capacitors being able to discharge during a switching cycle so that the input capacitors voltages can approach being fully discontinuous throughout the line cycle and bounded by a sinusoidal envelope.
- It should be noted that regardless of the input current shape, the input current harmonics complied with IEC 61000-3-2 Class A standards on harmonic content for both V_2 = 150 V and 500 V, as can be seen from Tables 3.1 and 3.2.



(a). V_2 = 150 V (b). V_2 = 500 V

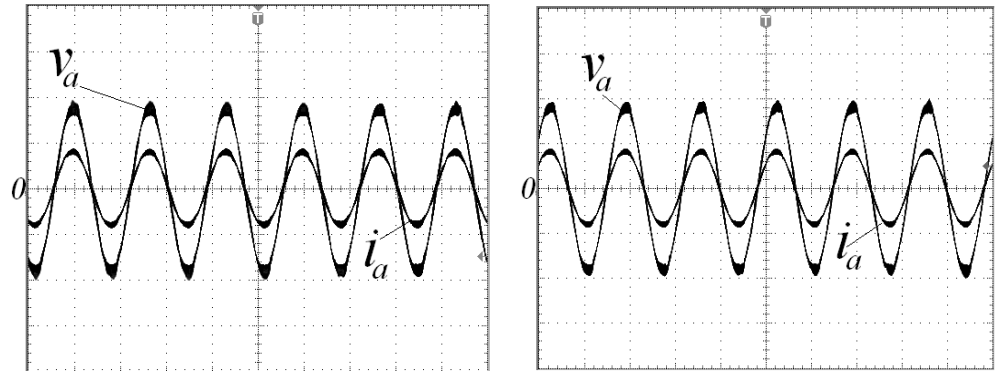
Fig 3.15: Input capacitor phase voltage for line cycles $P_{o,max}$ = 2 kW[V: 1200 V/div, t: 4 ms/div].



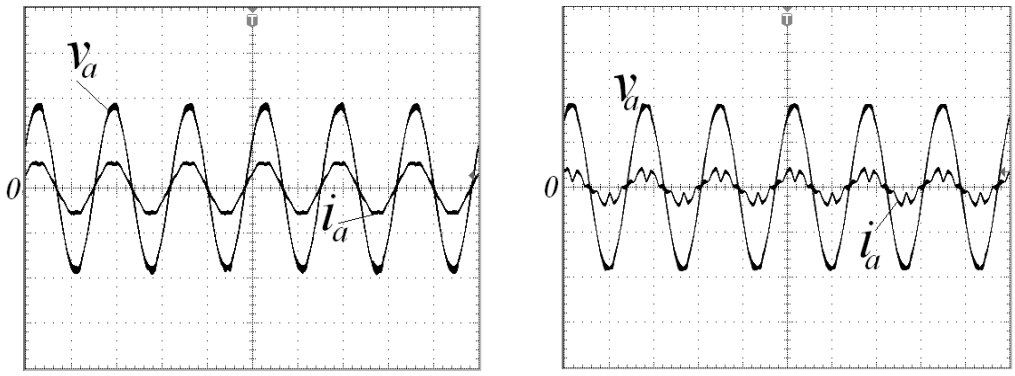
(a). V_2 = 150 V (b). V_2 = 500 V

Fig 3.16: Input capacitor phase voltage for line cycles $P_{o,max}$ = 2 kW [V: 750 V/div, t: 10 μs/div].

- Fig. 3.19 shows typical switch voltage and current waveforms for V_2 = 150 V and 500 V and P_o = 2 kW. It can be seen from Fig. 3.18(a) that the switch voltage (v_S) starts from zero and rises to a peak value whereas in Fig. 3.18(b), the v_S does not start from zero when the switch is turned off. This is because the v_S is dependent on the discharging of the input capacitors.
- In Fig. 3.19(a), v_S waveform is a result of the input capacitors having been completely discharged while the switch is on whereas in Fig. 3.19(b), v_S waveform is a result of the input capacitors not been fully discharged. The difference in switch voltage shapes corresponds to the fact that it is easier to discharge in the input capacitors when $D < 0.5$ than when $D > 0.5$ due to the presence of more current in the DC side in the former case. This is because the v_S is dependent on the discharging of the input capacitors.
- In Fig. 3.19(a), v_S waveform is a result of the input capacitors having been completely discharged while the switch is on whereas in Fig. 3.19(b), v_S waveform is a result of the input capacitors not been fully discharged. The difference in switch voltage shapes corresponds to the fact that it is easier to discharge in the input capacitors when $D < 0.5$ than when $D > 0.5$ due to the presence of more current in the DC side in the former case.



(a). P_o = 2000 W (b). P_o = 1500 W

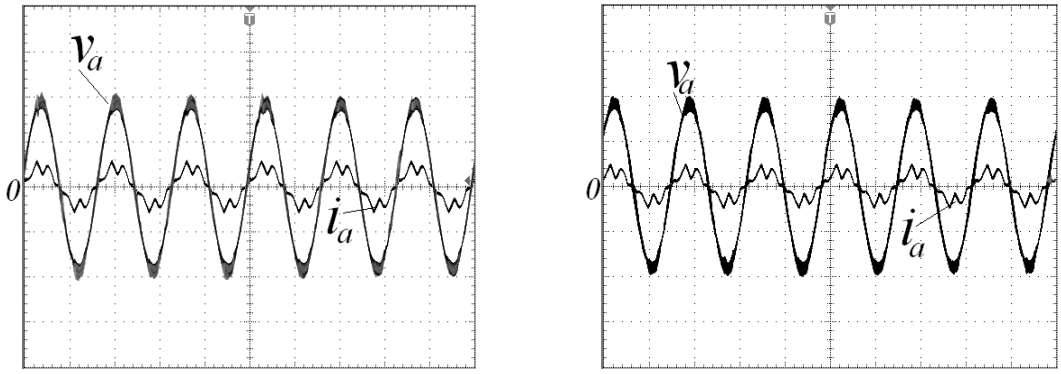


(c). P_o = 1000 W (d). P_o = 500 W

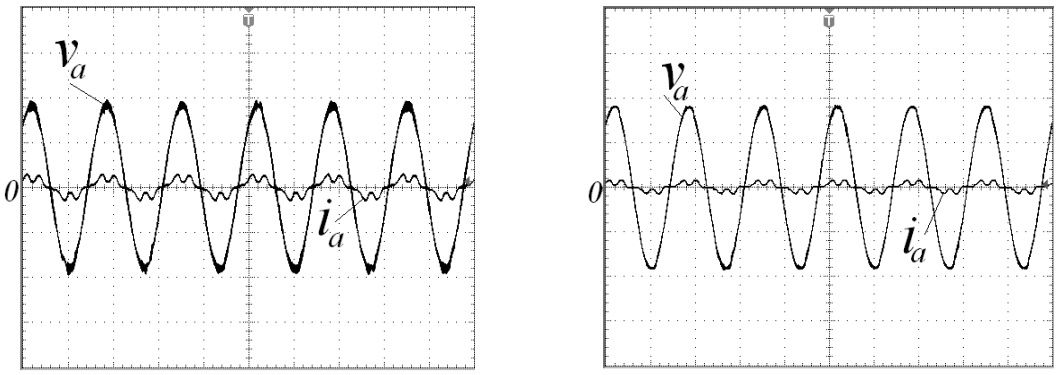
Fig 3.17: Input current and voltage when V_2 = 150 V [V: 100 V/div, I: 10 A/div, t: 10 ms/div].

Table 3.1 IEC 61000–3–2 Class A standard limits, harmonics of phase current for loads 2 kW–500W and PF when V_2 = 150V.

Harmonics	Class A	2kW	1.5kW	1kW	500W
5^{th}	2.06	0.17	0.14	0.09	0.68
7^{th}	1.39	0.03	0.02	0.06	0.54
11^{th}	0.6	0.08	0.07	0.06	0.17
13^{th}	0.38	0.09	0.07	0.05	0.09
PF		1.000	1.000	1.000	0.960



(a). P_o = 2000 W (b). P_o = 1500 W

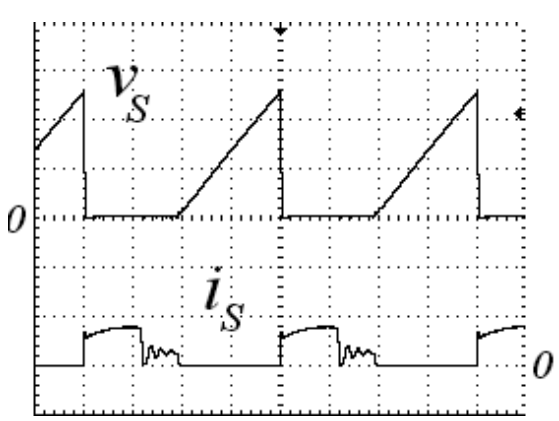


(c). P_o = 1000 W (d). P_o = 500 W

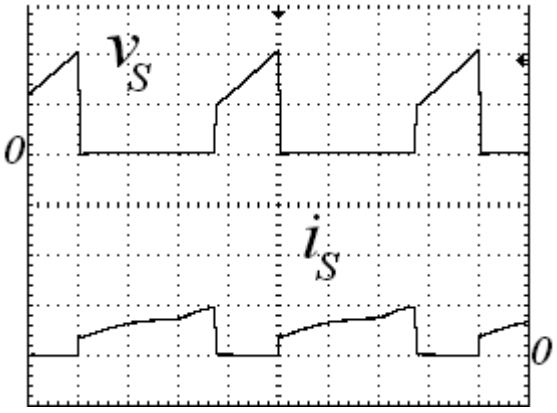
Fig 3.18: Phase current and voltage when V_2 = 500 V for loads [V: 100 V/div, I: 10 A/div, t: 10 ms/div].

Table 3.2: IEC 61000–3–2 Class A standard limits, harmonics of phase current for loads 2 kW–500W and PF when V_2=500 V

Harmonics	Class A	2kW	1.5kW	1kW	500W
5^{th}	2.06	1.04	1.05	0.93	0.67
7^{th}	1.39	0.83	0.87	0.50	0.30
11^{th}	0.6	0.14	0.18	0.05	0.08
13^{th}	0.38	0.07	0.18	0.04	0.01
PF		1.000	1.000	1.000	0.960



(a) [V: 250 V/div, I: 25 A/div, t: 10 µs/div]



(b) [V: 400 V/div, I: 10 A/div, t: 10 µs/div]

Fig 3.19: Switch voltage and current for V_2: (a) 150 V, (b) 500 V when $P_{o,max}$ = 2 kW.

- Fig. 3.20 shows curves of efficiency vs. load. It can be seen from these efficiency curves that the converter is more efficient when operating with V_2 = 500 V in boost mode that when it is operating in buck mode with V_2 = 150 V. This is because there is less current circulating in the converter when V_2 = 500 V and thus there are fewer conduction losses. It can also be seen in Fig. 3.19 that the switch current (i_S) has a different shape depending on whether V_2 = 150 V or V_2 = 500 V. In the former case, the input capacitors are fully discharged and when this happens, i_S level dips and corresponds to the input line current. This does not happen in the latter case because the input capacitors discharge until the switch is turned off, but their voltage never reaches zero due to partial discharge.

3.6 Conclusion

It was shown in Chapter 2 that it is possible to implement a single-switch three-phase AC-DC buck-boost converter with capacitive input filter, but although this converter is very attractive, it is also impractical because of its very high peak switch voltage stress. As a result, a new three-phase neutral point connected buck-boost multilevel converter with significantly reduced peak switch voltage stresses that is based on the single-switch converter was studied in this chapter. Moreover, the chapter examined how a reduced switched converter with capacitive input filter operates in the boost mode (conventional

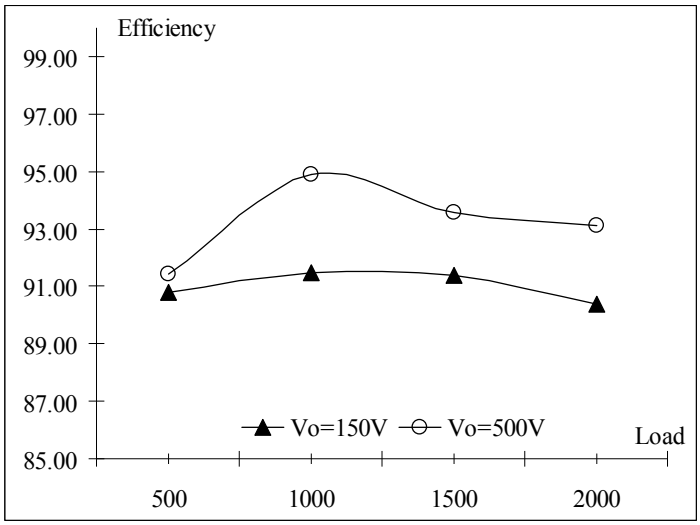


Fig 3.20: Efficiency curves buck mode boost mode at load conditions.

approach - a reduced switch input filter converter operating in the boost mode), which has not been previously addressed in the literature.

Chapter 4

4 A Three-Phase Neutral Point Connected Buck-Boost Quasi-Resonant Ac-Dc Converter

4.1 Introduction

The buck-boost converter that was the subject of Chapter 3 is an improvement over the conventional single-switch three-phase AC-DC buck-boost converter because it can be implemented with switches that have almost half the voltage rating of the switch that is needed for the conventional converter. Its switches, however, operate with what is known as "hard-switching" in the power electronics literature and this hard-switching operation results in switching losses. These switching losses can be reduced if the converter is operated with so-called "soft-switching" and the main focus of this chapter is the implementation of a particular soft-switching technique known as quasi-resonance to the buck-boost converter discussed in the previous chapter.

In this chapter, the terms "hard-switching" and "soft-switching" are defined and it is explained how soft-switching can reduce switching losses in power electronic converters. The new quasi-resonant buck-boost converter is then introduced and its general operation is explained, particularly the use of quasi-resonance (QR) as a soft-switching technique to reduce switching losses. The converter's modes of operation for both buck (voltage step down) mode and boost (voltage step up mode) are then discussed in detail and the analysis of the converter is presented. Based on the analysis, a design procedure that can be used for the selection of key components is developed, and then demonstrated with a design example. Finally, the feasibility of the new converter is confirmed with experimental results obtained from a prototype converter.

4.2 Soft-Switching

The switching of a switch (MOSFET / IGBT) is not ideal. If this switching was ideal, then a switch would turn on and off instantaneously and there would be no overlap between the voltage across a device and the current through it. In reality, however, such overlaps do exist whenever the device is in a switching transition, going from on-to-off or

vice versa. An example of the overlap of voltage and current that can be encountered by a device is shown in Fig 4.1 [1]. Since switching losses are related to the product of voltage and current during a switching transition, the overlap of voltage and current results in power losses. The switching loss of a switch is also related to its switching frequency – the faster a switch is turned on and off, the more switching losses are generated [36].

Switching losses, however, can be reduced if either the switch voltage or the current is made to be zero during a switching transition. Since the techniques for doing so involve making these transitions gradual (soft) instead of sudden (hard), they are known as soft-switching techniques in the power electronics literature. There are therefore two types of soft-switching techniques – zero-voltage-switching (ZVS) and zero-current-switching (ZCS). ZVS methods tend to be used in lower power converters where MOSFET devices are used and ZCS methods tend to be used in higher power converters where IGBTs tend to be used. The reasons why ZVS is preferred for MOSFETs and ZCS is preferred for IGBTs are due to the nature of the devices and will not be discussed in detail in this thesis.

Since the three-phase buck-boost converter discussed in Chapter 3 can be considered as a higher power converter, it is practically implemented with IGBTs; therefore, if it is to be implemented with soft-switching, then ZCS techniques should be considered. There are numerous possible methods by which ZCS can be implemented in this converter, but these methods generally fall into one of two categories – either they are quasi-resonant

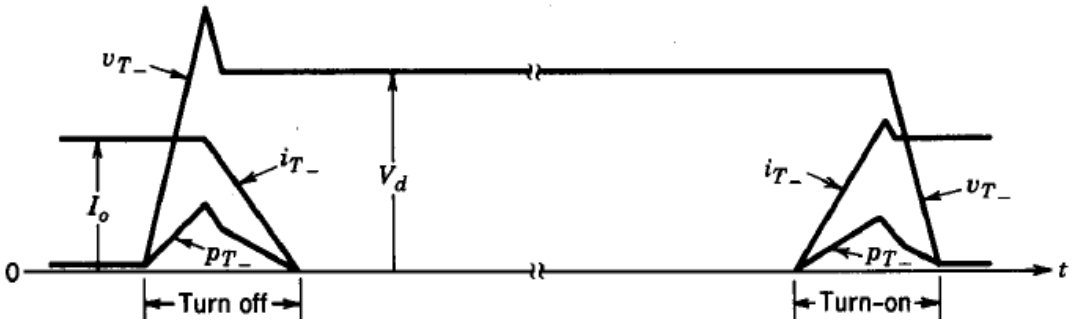


Fig 4.1: Non-ideal (hard) switching characteristics [1].

techniques [37]-[39] or they are zero-current transition (ZCT) techniques [40]-[42]. Both type of ZCS methods use a small inductor placed in series with a switch to slow down the rate of current rise when it is turned on. ZCT techniques typically use some sort of active auxiliary circuit containing a lower current rated switch to divert current away from a main converter switch whenever it is to be turned off while resonant type methods use resonant circuit elements placed in the converter to shape the switch current so that it falls to zero, thus enabling ZCS to occur.

In this chapter, the soft-switching of the buck-boost converter discussed in the previous chapter is considered with a quasi-resonant resonant-type ZCS method. This method gets the name "quasi-resonant" as the switch current waveforms are not fully resonant, which would mean sinusoidal switch currents. This quasi-resonant implementation was selected because it is the simplest and cheapest way by which ZCS operation can be achieved.

4.3 Operation of the Proposed Converter

The new three-phase, multilevel, quasi-resonant AC-DC converter is shown in Fig. 4.2. As can be seen from Fig. 4.2, its topology is the same as the converter in Chapter 3 except that components L_{q1}, C_{q1}, L_{q2} and C_{q2} have been added to the circuit. These components have a significant effect on the operation of the converter as they are the resonant elements that force the current in each switch to zero so that it can be turned off with ZCS – resonant components L_{q1} and C_{q1} force the switch current of switch S_1 to zero

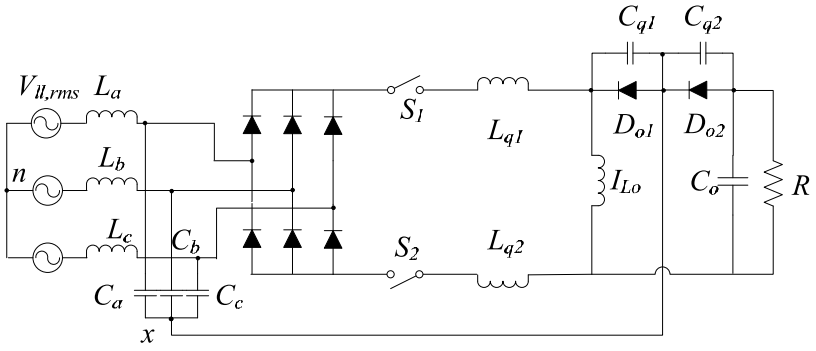


Fig 4.2: The proposed three-phase, multilevel, quasi-resonant buck-boost converter.

after it is turned on and resonant components L_{q2} and C_{q2} force the switch current of switch S_2 to zero after it is turned on.

Since the converter is a buck-boost converter, it can operate either in buck mode (step-down the output voltage with respect to the peak line-to-line input voltage) or in boost mode (step-up the output voltage with respect to the peak line-to-line input voltage). Similar to a conventional PWM DC-DC single-switch buck-boost converter, the proposed converter operates in buck mode when the switch duty cycle $D < 0.5$ and in boost mode when $D > 0.5$. In this section of the chapter the operation of the proposed converter when $D < 0.5$ and $D > 0.5$ are explained with modal equations.

The operation of the converter is explained in this section with reference to Figs. 4.3 and 4.5, which show equivalent circuit diagrams at the steady-state when $D < 0.5$ and when $D > 0.5$ respectively, and Figs. 4.4 and 4.6, which show typical converter waveforms for several switching cycles for $D < 0.5$ and $D > 0.5$ respectively.

4.3.1 $D < 0.5$ [Buck mode of operation]

During the buck mode of operation, prior to $t = t_0$, both switches S_1 and S_2 are off; therefore the AC and DC sides are separated. The input capacitors are charged by the line currents. In the DC side, the output inductor current (I_{Lo}) freewheels through output diodes D_{o1} and D_{o2}. The initial conditions for the resonant components are zero ($i_{Lq,k(t0)} = 0$, $v_{Cq,k(t0)} = 0$) and the initial voltage of C_a is $v_{Ca,k(t0)}$.

Mode 1 ($t_0 < t < t_1$), [Fig. 4.3(a)]:

S_1 is turned on and current $i_{Lq,k}$ gradually increases due to the presence of inductor L_{q1} in the conduction path. As a result of the gradual rise in $i_{Lq,k}$, C_a continues to be charged by the difference current $I_{a,k} - i_{Lq,k}$; thus the voltage of C_a ($v_{Ca,k}$) starts to decrease when $i_{Lq,k}$ becomes greater than $I_{a,k}$. C_b and C_c charge using respective line currents $I_{b,k}$ and $I_{c,k}$. [$I_{a,k} = -(I_{b,k} + I_{c,k})$] throughout Mode 1. As $i_{Lq,k}$ increases, the current through D_{o1} decreases and the voltage of C_{q1} ($v_{Cq,k}$) remains zero.

The voltage across L_{q1} equals $v_{Ca,k}$ because the current of L_o is freewheeling through L_o, D_{o1}, D_{o2} and R; thus output voltage V_o is cancelled by the voltage across L_o. The rate

of rise of current of L_{q1} can be written as the ratio between the voltage across L_{q1} and the inductance L_{q1} as

$$\frac{di_{Lq,k}}{dt} = \frac{v_{Ca,k} - v_{Cq,k}}{L_q} = \frac{v_{Ca,k}}{L_q} \tag{4.1}$$

where $di_{Lq,k}/dt$ is the rate of rise of L_{q1} current and $v_{Ca,k}$ and $v_{Cq,k}$ are the instantaneous voltages across C_a and C_{q1} in the k^{th} switching cycle.

$$\frac{dv_{Ca,k}}{dt} = \frac{I_{a,k} - i_{Lq,k}}{C_a} \tag{4.2}$$

The variation in the voltage across C_a can be written as the ratio between the difference current ($I_{a,k}$ - $i_{Lq,k}$) and the capacitance C_a as given in Eq. (4.2). This mode ends at $t = t_1$ when $i_{Lq,k(t1)}$ is equal to the current of L_o.

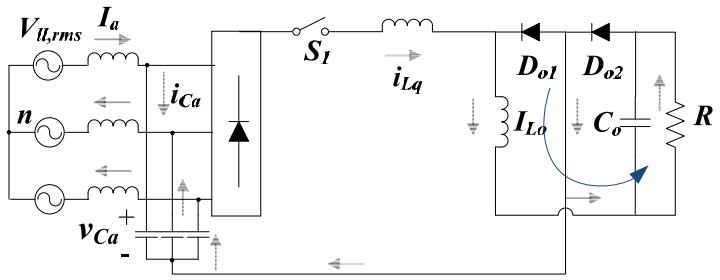
Mode 2 ($t_1 < t < t_2$), [Fig. 4.3(b)]:

Mode 2 begins when $i_{Lq(t1)}$ is equal to the current of L_o. L_{q1} and C_{q1} begin to resonate while D_{o1} stops conducting. C_a continues to discharge, according to Eq. (4.2). The current of L_{q1} is increasing and the difference current ($i_{Lq,k}$ - I_{Lo}) charges C_{q1}. The resonance between L_{q1} and C_{q1}, the components associated with soft switching of S_1, can be described as follows:

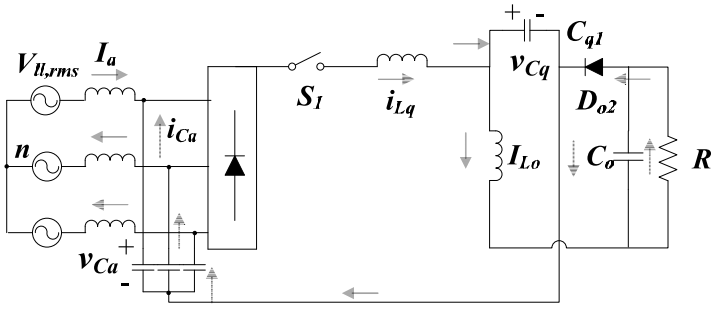
$$\frac{di_{Lq,k}}{dt} = \frac{v_{Ca,k} - v_{Cq,k}}{L_q} \tag{4.3}$$

$$\frac{dv_{Cq,k}}{dt} = \frac{i_{Lq,k} - I_{Lo}}{C_q} \tag{4.4}$$

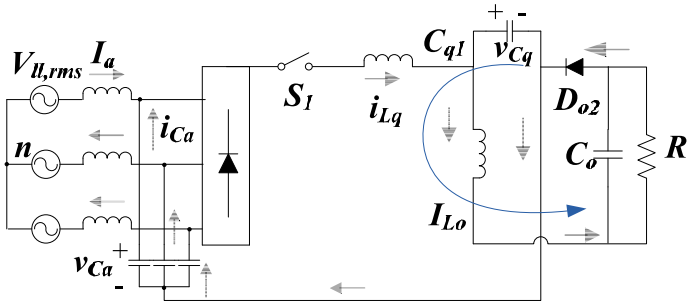
Eq. (4.3) gives the rate of rise of current of L_{q1} and Eq. (4.4) gives the rate of rise of voltage of C_{q1}. $i_{Lq,k}$ reached its peak during this mode and then becomes equal to the current of L_o at the end of this mode.



(a) Mode 1($t_0 < t < t_1$)

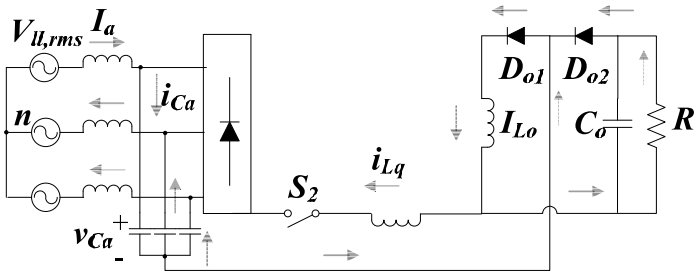


(b) Mode 2($t_1 < t < t_2$)

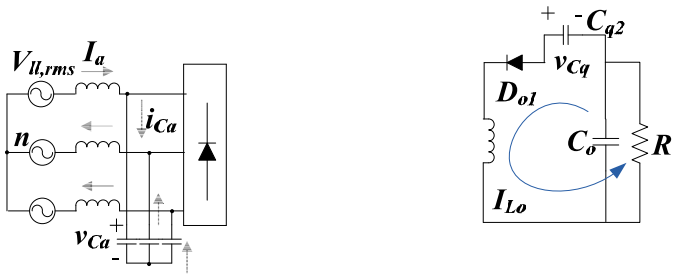


(c) Mode 3($t_2 < t < t_3$)

(d) Mode 4($t_3 < t < t_4$)



(e) Mode 5($t_4 < t < t_5$)



(f) Mode 6($t_5 < t < t_6$)

Fig 4.3: Modes of the converter when $D < 0.5$.

Mode 3 ($t_2 < t < t_3$), [Fig. 4.3(c)]:

At the start of this mode $i_{Lq,k}$ equals the current of L_o and continues to decrease. $i_{Lq,k}$, however, is still greater than $I_{a,k}$, the phase A current; therefore, C_a continues to discharge (or charge in the opposite direction). C_a begins to charge when $i_{Lq,k} < I_{a,k}$. Finally, when i_{Lq1} has fallen to zero, C_a charges using the entire phase A current $I_{a,k}$. Modal Eqs. (4.1) - (4.3) prevail during this mode.

Mode 4 ($t_3 < t < t_4$), [Fig. 4.3(d)]:

At $t = t_3$, Mode 4 begins when the current of L_{q1} has decreased to zero [$i_{Lq,(t3)} = 0$]. S_1 can be turned off with ZCS when this happens as there is no overlap of switch voltage and current. C_a charges linearly using the entire phase A current $I_{a,k}$ as follows:

$$V_{Ca,k(t4)} = V_{Ca,k(t3)} + \frac{I_{a,k}}{C_a}(t_4 - t_3) \tag{4.5}$$

where $V_{Ca,k(t4)}$ and $V_{Ca,k(t3)}$ are the voltage values of C_a at $t = t_4$ and $t = t_3$ respectively. C_{q1} discharges linearly as the entire current of L_o (which is assumed to be equal to the average current value I_{Lo}) is provided by C_{q1}, according to

$$V_{Cq,k(t4)} = V_{Cq,k(t3)} - \frac{I_{Lo}}{C_q}(t_4 - t_3) \tag{4.6}$$

where $V_{Cq,k(t4)}$ and $V_{Cq,k(t3)}$ are the voltage values of C_{q1} at $t = t_4$ and $t = t_3$ respectively. C_{q1} eventually discharges sometime during this mode.

Mode 5 ($t_4 < t < t_5$), [Fig. 4.3(e)]:

Mode 5 starts when S_2 is turned on. It does so with ZCS as the rate of rise of current is gradual because inductor L_{q2} is in series with S_2. Since there is a 180º phase shift between turn-on time of the two switches, $t_4 = t_0 + T_s/2$, where T_s is the switching period.

As $i_{Lq,k}$ gradually increases (equivalent to Mode 1), the current flowing through D_{o2} gradually decreases. When $i_{Lq,k}$ has risen to the level of the output current of L_o, L_{q2} begins to resonate with C_{q2}. The current of L_{q2} $i_{Lq,k}$ rises, reaches its peak and then decreases while the voltage of C_{q2} increases.

C_b and C_c begin to discharge when $i_{Lq,k}$ starts to increase above the output current of L_o to supply the increasing resonant current (equivalent to Modes 2-3). This mode ends when C_{q2} reaches its peak voltage ($V_{Cq,k(t2)}$) and when i_{Lq2} has fallen to the level of the output current of L_o.

Mode 6 ($t_5 < t < t_6$), [Fig. 4.3(f)]:

Mode 6 starts at $t = t_5$, when $i_{Lq,k} = 0$ and S_2 can be turned off with ZCS. Mode 6 is similar to Mode 4 except that C_{q2} discharges into the load instead of C_{q1}. Sometime during this mode, C_{q2} becomes completely discharged and thus D_{o2} begins to conduct the entire load current.

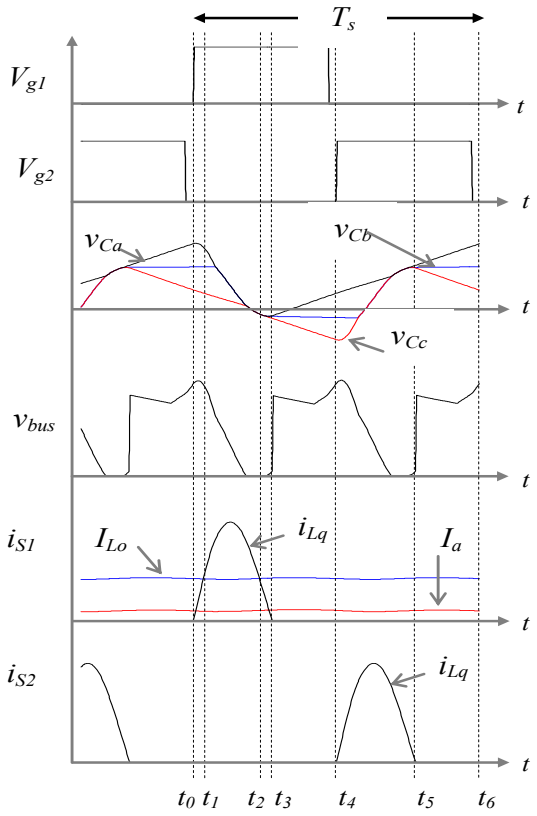


Fig 4.4: Typical waveforms when $D < 0.5$.

Mode 6 ends when S_1 is turned on at $t = t_6$, with ZCS. This is the start of a new switching cycle, (k+1). Modal equations for Mode 5 and 6 are not given as they are same as the Eqs. derived for Modes 1-4.

The ZCS nature of the converter can be seen in the typical converter waveforms shown in Fig. 4.4. It can be seen how both switch currents (I_{Lq1} and I_{Lq2}) resemble a hump that begins at zero and ends at zero. This resonant hump is caused by the resonant components that are associated with each switch and it is their presence in the converter that allows the switch currents to be shaped in this manner to allow for ZCS operation.

4.3.2 $D > 0.5$ [Boost mode of operation]

The steady-state modes the converter goes through during the boost mode of operation are shown in Fig. 4.5 and the typical waveforms are given in Fig. 4.6. During boost

operation, at least one of the switches is on at all times whereas there are instances where none of the switches are on when the converter is in the buck mode. Since the proposed converter is a QR ZCS converter, however, a switch can be on without any current through it as it is extinguished before the switch is turned off. As a result, the steady-state operation of the converter in the boost mode is very similar to its operation in the buck mode and only the modal equations that are different in a particular mode are stated below. It should also be noted that if a switch is on, but there is no current through it, it is shown transparent in the circuit diagrams.

Prior to $t = t_0$, S_2 is on, but the current through L_{q2} ($i_{Lq,k,(t0)}$) is zero; thus, the only differences that boost mode of operation has with buck mode are the discharging of C_{q2} in the DC side and the initial voltage across C_{q2} at $t = t_0$, which is $v_{Cq,k(t0)}$.

Mode 1 ($t_0 < t < t_1$), [Fig. 4.5(a)]:

At $t = t_0$, S_1 is turned on, with ZCS. C_{q2} continues to discharge linearly as the output inductor current (which is assumed to be equal to its average value I_{Lo}) flows through it. This discharging can be expressed as

$$V_{Cq,k(t1)} = V_{Cq,k(t0)} - \frac{I_{Lo}}{C_q}(t - t_0) \tag{4.7}$$

where $V_{Cq,k(t1)}$ and $V_{Cq,k(t0)}$ are voltages of Cq2 at $t = t_0$ and $t = t_1$ respectively.

During Mode 1, L_{q1} resonates with C_a, but does not interact with C_{q2}, as is the case for Mode 1 when $D < 0.5$ and the converter is operating in the buck mode; therefore, the equations stated for Mode 1 when $D < 0.5$ are still valid. $i_{Lq,k}$ is given by Eq. (4.1) and $v_{Ca,k}$ is given by (4.2). Mode 1 ends when the current of L_{q1} equals average current of L_o at $t = t_1$, $I_{Lq1,k(t1)} = I_{Lo}$.

Mode 2 ($t_1 < t < t_2$), [Fig. 4.5(b)]:

At $t = t_1$, C_{q1} begins to charge as C_{q1} and L_{q1} starts to resonate. C_{q2} continues to discharge linearly as the output inductor current flows through it. As a result, the net

charging current through C_{q1} is ($i_{Lq,k}$ - I_{Lo}), which is same as the charging current during Mode 2 when the converter is operating in the buck mode ($D < 0.5$). During Mode 2, C_a discharges because $i_{Lq1} > I_{a,k}$ and the additional resonant current must be supplied by C_a. Sometime during this mode, S_2 is turned off with ZCS (switch S_2 current was extinguished prior to $t = t_0$). Eqs. (4.2) - (4.4) give the behavior of $v_{Ca,k}$, $i_{Lq,k}$, and $v_{Cq,k}$ (voltage of C_{q1}) whereas voltage of C_{q2} is given by Eq. (4.7).

Mode 3 ($t_2 < t < t_3$), [Fig. 4.5(c)]:

Mode 3 begins when $i_{Lq,k}$ starts to decrease the output current of L_o; as a result, C_{q1} begins to bridge the gap between currents I_{Lo} and $i_{Lq,k}$. C_{q2} is fully discharged during this mode, which ends when $i_{Lq,k(t3)} = 0$. The converter acts the same as in Mode 3 for buck mode of operation, as described above.

Mode 4 ($t_3 < t < t_4$), [Fig. 4.5(d)]:

At the beginning of Mode 4, C_a begins to be charged by the entire phase A current $I_{a,k}$ as $i_{Lq,k(t3)} = 0$. C_{q1} is linearly discharged by the output inductor current according to

$$V_{Cq,k(t4)} = V_{Cq,k(t3)} - \frac{I_{Lo}}{C_q}\left(t_4 - t_3\right) \tag{4.8}$$

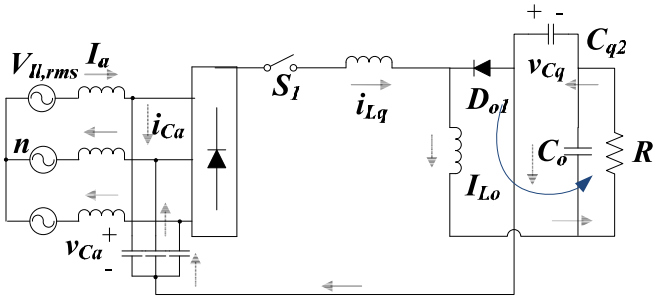
where $V_{Cq,k(t3)}$ is the voltage of C_{q1} at $t = t_3$ and $V_{Cq,k(t4)}$ is the same at $t = t_4$.

Mode 5 ($t_4 < t < t_5$), [Fig. 4.5(e)]

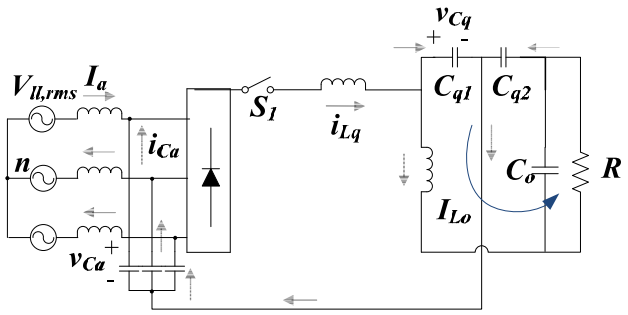
S_2 is turned on with ZCS at $t = t_4$. The switch current of S_1 is zero and S_1 is turned off at $t = t_0 + DT_s$. It should be noted that during Mode 5, both switches will be on for some time until S_1 is turned off; however only S_2 will be conducting as the current in S_1 is extinguished during Mode 4.

C_a continues to charge linearly while C_b and C_c both stop charging and begin to discharge, supplying the increasing current of L_{q2} ($i_{Lq,k}$). C_{q2} starts to charge when $i_{Lq,k}$ is greater than the current of L_o. During this mode, $i_{Lq,k}$ completes its resonant cycle and becomes zero; thereafter C_b charges using phase B current $I_{b,k}$ and C_c charges using phase

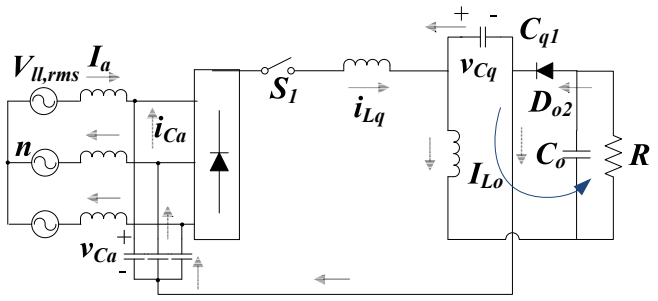
C current $I_{c,k}$. Thereafter, C_{q2} is discharged by the output inductor current. This mode ends when S_1 is turned on at $t = t_5$ ($= t_0 + T_s$) and a new switching cycle ($k + 1$) begins.



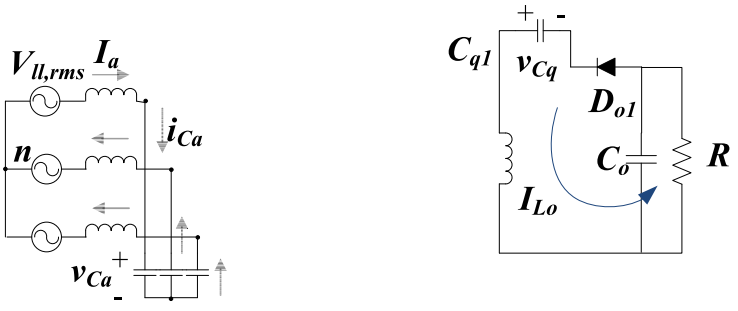
(a) Mode 1($t_0 < t < t_1$)



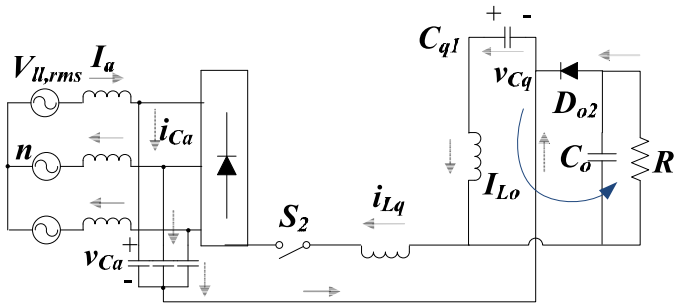
(b) Mode 2($t_1 < t < t_2$)



(c) Mode 3($t_2 < t < t_3$)



(d) Mode 4($t_3 < t < t_4$)



(e) Mode 5($t_4 < t < t_5$)

Fig 4.5: Modes of the converter when $D > 0.5$.

4.4 Mathematical Analysis

The ultimate objective of the analysis is to determine steady state converter operating points for various combinations of converter components. The results of the analysis will then be used to design the converter so that it can operate with an appropriate input current harmonic content and with quasi-resonant zero-current-switching (ZCS) for a desired operating range (range of output voltage, output load).

For the analysis of the converter, the following assumptions are made:

- The line frequency (f_l) is smaller than the switching frequency (f_s); therefore, the line currents can be considered to be constant for all the modes (e.g. phase A current $I_{a,k}$) of any selected switching cycle k.

- Output inductor L_o is sufficiently large to be considered as a current source of value I_{Lo}, where I_{Lo} is the average current through L_o, and C_o is sufficiently large to be considered as a voltage source V_o, where V_o is the output voltage.

- The value of all three input capacitors are the same of that $C_a = C_b = C_c$; therefore, only the voltage of C_a v_{Ca}, is considered throughout this chapter as v_{Cb} and v_{Cc} are the same as v_{Ca} but with phase shifts of 120º and 240º respectively.

- Resonant components $L_{q1} = L_{q2} = L_q$ and $C_{q1} = C_{q2} = C_q$; therefore, only the current of L_{q1} and voltage of C_{q1} are obtained in this chapter as the current of L_{q2} and the voltage of C_{q2} can be derived from L_{q1} and C_{q1} respectively. The currents through each resonant inductor is indicated as $i_{Lq,k}$ and the voltage across each resonant capacitor is indicated as $v_{Cq,k}$.

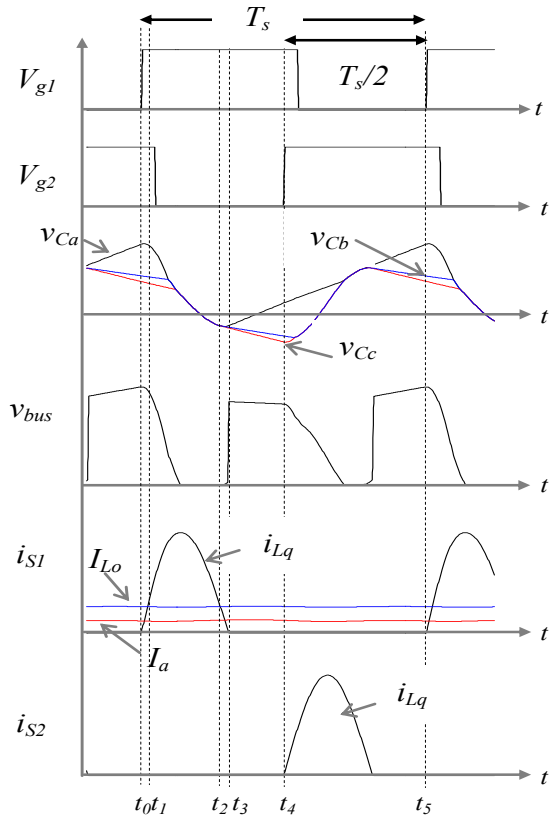


Fig 4.6: Typical waveforms when $D > 0.5$.

- For both buck and boost operations, the gating signals of switches S_1 and S_2 are the same, but shifted 180° with respect to each other.

- Due to the symmetry of a three-phase system, only 1/6th of the line cycle needs to be considered in the analysis. For the analysis presented in this chapter, a line cycle interval of [π/2-2π/3] is chosen, which means that for the first switching cycle, the phase A voltage is at its peak value $V_{a,k} = V_m$ and the voltages of phases B and C are $V_{b,k} = V_{c,k} = - V_m/2$, where $V_{a,k}$, $V_{b,k}$, $V_{c,k}$ are voltages of phases A, B and C and V_m is the peak phase voltage. It should be noted that the selection of this particular 1/6th of the line cycle interval is arbitrary and any portion could have been chosen.

4.4.1 Quasi-Resonant Criterion

The first condition that needs to be examined is whether a resonant inductor current (i_{Lq}) falls to zero before its corresponding switch is turned off. The instantaneous value of i_{Lq} is almost the same for every switching cycle; therefore if i_{Lq} is zero before the end of switch on-time $t_{on} = D/f_s$, then the ZCS condition is met. This can be checked by the following equation:

$$I_{Lq,k(t_0+D/f_s)} = \int_{t_0}^{(t_0+D/f_s)} \frac{v_{Ca,k} - v_{Cq,k}}{L_q} dt + I_{Lq,k(t0)} = 0 \qquad (4.9)$$

where $I_{Lq,k(t0+D/fs)}$ is the inductor L_{q1} current at the time of switch turn-off, $I_{Lq,k(t0)}$ is the initial current, $v_{Ca,k}$ and $v_{Cq,k}$ are the instantaneous voltages of C_a and C_{q1} respectively. If $I_{Lq,k(D/fs)}$ equals zero, that means the switch current is extinguished by the time the switch is turned off. If this condition is not satisfied, the resonant components and the switch on-time ($t_{on} = D*1/f_s$) must be changed.

4.4.2 Steady-State Criterion

When the converter is in steady-state, the average current through a capacitor and the average voltage across an inductor must be zero during a line cycle. The steady state condition of the converter for a selected combination of component and parameter values can thus be tested by determining the average current of any input capacitor. If this is

zero, then the converter is operating in steady-state. Due to symmetry, it is sufficient to check just $1/6^{th}$ of the line cycle to determine whether the converter is operating in steady-state.

The line interval - [$\pi/2$-$2\pi/3$] is considered; thus the first switching cycle, the phase A voltage is at its peak value $V_{a,k} = V_m$ and the voltages of phases B and C are $V_{b,k} = V_{c,k} = -V_m/2$, and the phase A current is at its peak value $\left(I_{a,k} = 2P_o/3V_m\right)$. Using the intial conditions and modal Eqs. 4.2, 4.4 and 4.5, $v_{Ca,k}$ can be found for the first switching cycle k; then by taking the final mode variable values as the initial conditions, $v_{Ca,(k+1)}$ can be found. By sweeping over the entire line interval in this manner, v_{Ca} waveforms can be determined. Since the current of C_a is the product of C_a and the integral of v_{Ca}, therefore, the average value of the current through C_a, $I_{Ca(ave)}$ can be determined as follows:

$$I_{Ca(ave)} = \frac{1}{6}\frac{\sum_{k=1}^{n_{sw}}\int_{t_0}^{t_6}\left(dv_{Ca,k}\right)dt}{\left(1/f_l\right)} \tag{4.10}$$

where t_0 is the start time of Mode 1, t_6 is the end time of k^{th} switching cycle and $v_{Ca,k}$ is the instantaneous voltage across capacitor C_a. This equation must have a value of zero when the converter is operating in steady-state.

If $I_{Ca(ave)}$ is not zero, however, then circuit parameters such as C_a, L_q, C_q, f_s and/or D must be changed until Eq. (4.9) is satisfied. Any combination of components that satisfies Eq. (4.9) will result a set of components that allow the converter operate in the steady-state. After checking the steady-state condition of the converter, the final criterion to check is whether the phase currents meet IEC standard or not as explained below.

4.4.3 Input Power Factor Correction (PFC) Criterion

As explained in [43], if the input capacitors (e.g. C_a) are chosen to be sufficiently small, then they can operate in the discontinuous voltage mode (DVM) with their voltages becoming zero sometime within each switching cycle. The input capacitor phase voltages (e.g. v_{Ca}) then consist of trains of triangular pulses with peaks that naturally track a sinusoidal shape, which minimizes the presence of low frequency harmonics.

Since the input capacitor voltages consist of a fundamental component and high frequency components when they are discontinuous and the input voltages can be considered to be purely sinusoidal, the input line currents can be sinusoidal as the input inductors can filter the high frequency components.

This can be checked by performing a Fast Fourier Transform to the phase currents ($FFT\{i_a\}$). To find the phase current, i_a, the instantaneous input capacitor phase voltage (e.g. $v_{Ca,k}$) must be tracked, then, based on $v_{Ca,k}$ and the sinusoidal input phase A voltage, the voltage across an input inductor L_a can be found ($v_{La,k}$). Based on $v_{La,k}$, the instantaneous current of L_a, $i_{La,k}$, can be obtained and the Fast Fourier Transform can be performed to check if the IEC 61000-3-2 Class A standard is met. If the IEC standard is not met, then a much smaller C_a must be selected and all three criteria must be rechecked.

To find the instantaneous values for parameters such as $v_{Ca,k}$, $i_{Lq,k}$, etc. for the k^{th} switching cycle, the process should start with some initial values ($V_{Ca,k(t0)}$, $I_{a,k}$) for Mode 1. Based on the modal Eqs. presented above, the variable values at the end of Mode 1 (e.g. $V_{Ca,k(t1)}$) can be calculated and then considered as the initial conditions for Mode 2. The values at $t = t_2$ can be found using the modal equations that define Mode 2, the values at $t = t_3$ can be found using the modal equations that define Mode 3 and so on until the end of the k^{th} switching cycle is reached. After the program checks whether the variable values for one whole switching cycle has been calculated ($t_6 = t_0 + T_s$), the values of the next switching cycle can be derived based on the final variable values for k^{th} switching cycle (i.e. $V_{Ca,k(t6)} = V_{Ca,k+1(t0)}$). This process is repeated until all the switching cycles for one line cycle are obtained by iterating $k = f_s/f_l$ times.

The converter is a buck-boost converter and thus should satisfy the above criteria over a wide range of output voltages (V_o) and power levels (P_o). Since it is a quasi-resonant converter, the converter needs to be operated with variable switching frequency f_s with a fixed switch on-time ($t_{on} = D/f_s$) and a variable off-time [44]. The switch on-time needs to be fixed because of the timing associated with the switch current – the converter's resonant components shape the switch current so that it can falls to zero, which allows the switch to be turned off with ZCS. If the switch on-time is varied, then this ZCS

opportunity can be missed - if the switch is turned off too soon, then the switch will be turned off while current is flowing through it, or if the switch is turned off too late, then again the switch will be turned off while current is flowing through it as current will have started to flow in the switch after settling at zero for some time.

Since the converter's output voltage is dependent on the switching frequency f_s, it must be sufficiently large to ensure that the converter can operate with the desired output voltage over the entire load range. This is especially true when the converter operates as a buck converter and its maximum duty cycle (D) is limited to 0.5 as it cannot step up voltage.

Due to the wide range of V_o - P_o combinations, however, the switching of the converter should be implemented by some combination of variable-frequency and constant-frequency PWM mechanisms. The switching frequency (f_s) can be controlled in the range between full load and light load. In this power range the f_s can be made to vary from some upper frequency, $f_{s,h}$ to some lower frequency $f_{s,l}$, that should be just above 20 kHz, which just above the audible range.

The analysis can proceed according to the following steps:

- **Step 1:** Start the analysis by assuming $D = 0.5$ and $f_s = 50$ kHz (where $f_{s(max)}$ for the converter is set at 50 kHz) for the case when the converter operates as a buck converter with full load.
- **Step 2:** Select the combination of component values for C_a, L_q, and C_q to be considered.
- **Step 3:** Using the modal equations in Section 4.3, check the validity of the operating point by checking whether the three criteria: the ZCS turn-off criterion, steady-state condition, and the input PFC criterion - given above are met.

  Since the variables are interdependent, a closed form solution cannot be derived and some sort of a computer program is required. One way of writing such a program is shown in Fig. 4.7. Fig. 4.7 shows a flowchart that was used to develop a computer program that checks to see if the selected operating point (C_a, L_q, C_q) and parameters (D, f_s) satisfy the three criteria.

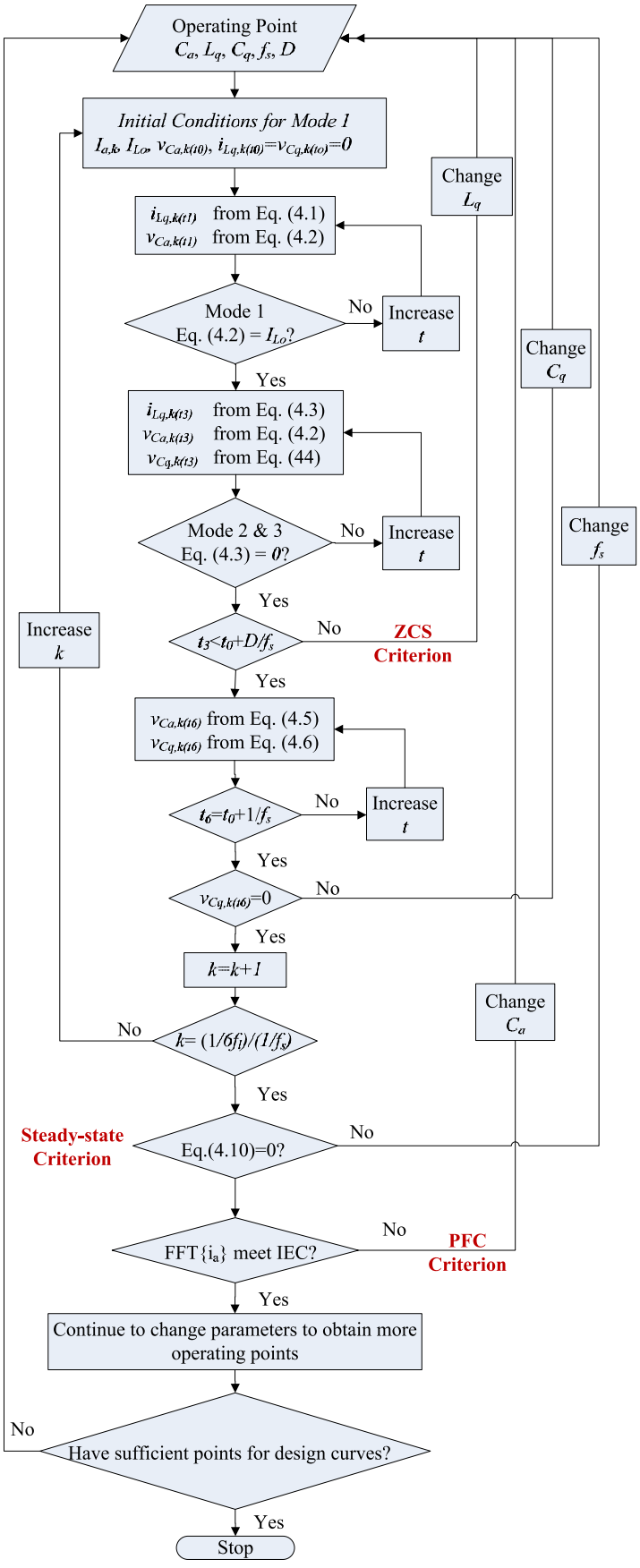


Fig 4.7: Flowchart to select operating points.

- **Step 4:** Considering the particular program whose flowchart is shown in Fig. 4.7, begin by assuming some initial conditions for Mode 1 of switching cycle k = 1, defined as when $V_{a,k} = V_m$ and $V_{b,k} = V_{c,k} = -V_m/2$.
- **Step 5:** Solve modal Eqs. (4.1) and (4.2) to find the values of $v_{Ca,k}$ and $i_{Lq,k}$ ($v_{Ca,k(t0)}$, $_{iLq,k(t0)}$) at the end of Mode 1. These values are then used as initial conditions for Mode 2 and the values at the end of Mode 2 are used as the initial conditions for Mode 3, etc. In this way, the program can sweep through all the modes for the k^{th} cycle and then proceed to $(k+1)^{th}$ switching cycle. The loop ends when $k = (1/f_l)/(1/f_s)$, when a complete line cycle has been checked, at which point, it can be determined if the three criteria are met. If the three criteria have not been met, then D or f_s or both must be changed and the program must go through the same steps until they are met.
- **Step 6:** Once an operating point for full load operation when the converter is in buck mode is selected, then the switch on-time ($t_{on} = D/f_s$) can be determined and suitable D and f_s combinations for other V_o/P_o conditions can be found.
- **Step 7:** By repeating Step 5, it can be checked if the selected operating point for buck mode full load operation is also valid for other conditions such as buck light load, boost full load and boost light load etc. If not, the above steps must be repeated until such point is found.

4.5 Design and Example

In this section of the chapter, a procedure that can be used to determine the key parameters of the proposed converter (the input capacitors, input inductors, and resonant components) is presented and demonstrated with an example. For this example, the converter specifications are as follows: input line-line rms voltage V_{in} = 220 V, output voltage V_o = 150 V (buck $D < 0.5$) and 500 V (boost $D > 0.5$), maximum output power P_o = 2 kW.

A. Selecting the Input Capacitors ($C_a = C_b = C_c$), Switching Frequency (f_s) and Duty Cycle (D)

In order to select an input capacitor value (C_a), either the buck or the boost mode of operation and full load or minimum load should be considered first and converter operation should be confirmed for the other output voltage (V_o) and output power (P_o) combinations. The selected operating point should be in steady-state, ensure that the input capacitors are in discontinuous voltage mode (DVM) and ensure that the switches operate with zero current switching (ZCS). Design curves shown in Figs. 4.8 were plotted using the modal equations and the computer program derived in the previous section of this paper.

For this example, the switching frequency (f_s) is made to vary in the range between 55 kHz at full load and 20 kHz at light load where light load is 500 W. When f_s is less than to 22 kHz, the constant-frequency PWM is used to regulate the output voltage without decreasing f_s further. A lower limit of 22 kHz is considered as it is just above the audio range of frequencies.

Step 1 of selecting C_a is to consider when the converter is at buck full load operation (V_o = 150 V, P_o = 2 kW) and find components and switch on-time (t_{on}) such that the required voltage gain (steady-state) and the input PFC is obtained. Once suitable value of C_a and D/f_s are found, curves such as those shown in Fig. 4.8(a) can be drawn. This process can then be extended to other V_o/P_o combinations such as V_o = 150 V, P_o = 500 W, V_o = 500 V, P_o = 2 kW and V_o = 500 V, P_o = 500 W to obtain similar design curves shown in Figs. 4.8(b), 4.8(c), 4.8(c) respectively.

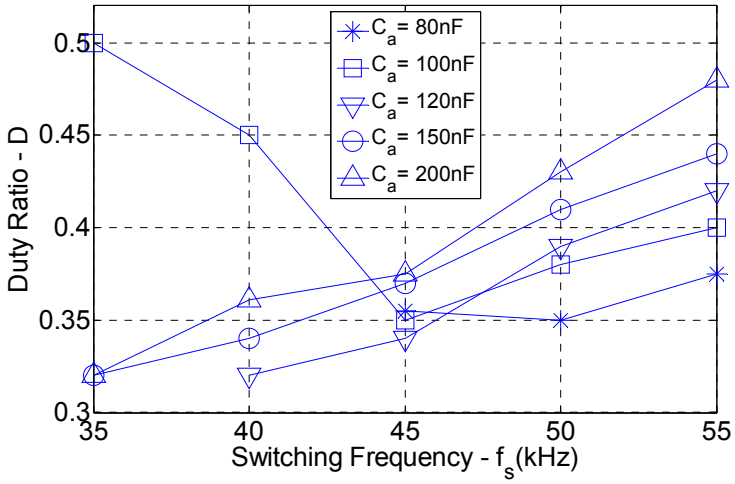
Then in Step 2, an input capacitance that can meet the design criteria for all output combinations is found so that the on-time t_{on} is constant. It should be noted that determining a suitable value for C_a is an iterative process and only the final iteration of this process is shown below.

Step 1: Finding suitable C_a, f_s, D for V_o = 150 V, P_o = 2 kW

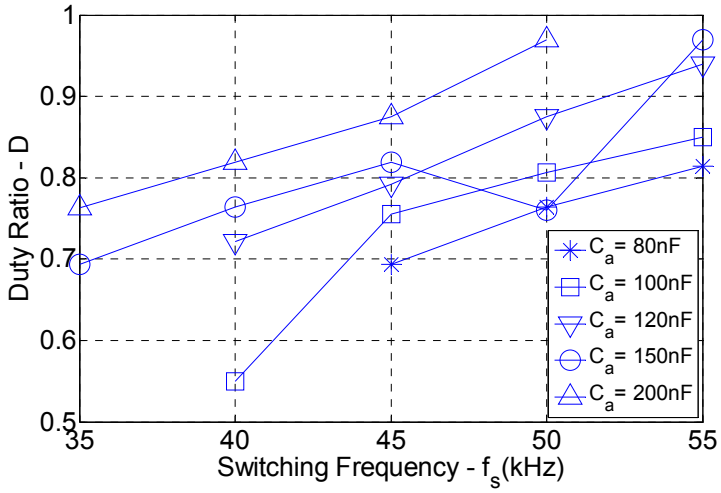
As mentioned above, the objective of this step is to find suitable combinations of C_a - f_s - D so that the required voltage gain at steady-state and DVM of C_a are obtained. The four plots shown in Fig. 4.8 show suitable operating points for buck full load (V_o = 150 V, P_o = 2 kW), buck light load (V_o = 150 V, P_o = 500 W), boost full load (V_o = 500 V, $V_o P_o$ = 2kW), and boost light load (V_o = 500 V, P_o = 500 W). It is assumed that if C_a can be found to satisfy the design criteria at the boundaries of V_o/P_o [e.g. (V_o = 150 V, P_o = 2 kW and (V_o = 500 V, P_o = 500 W)], then C_a will be suitable value for operation within the boundaries. In each subplot of Fig. 4.8, f_s and D are shown on the x and y axes respectively and each curve represents a particular C_a value. These values can be found using the modal equations and the computer program mentioned in the previous section.

When the converter operates as a buck converter (V_o = 150 V), D can only vary between 0 and 0.5. When the converter is operated as a boost converter, it can only vary between 0.5 and 1. For the given converter specifications, C_a is considered between 80 nF and 200 nF; if C_a is too small (< 80 nF) then voltage regulation becomes difficult and $M = V_o/V_{ll(pk)}$ will be less than the required value especially for buck operation. On the other hand if C_a is too large (> 200 nF) then the DVM operation of C_a becomes difficult, especially for light load conditions.

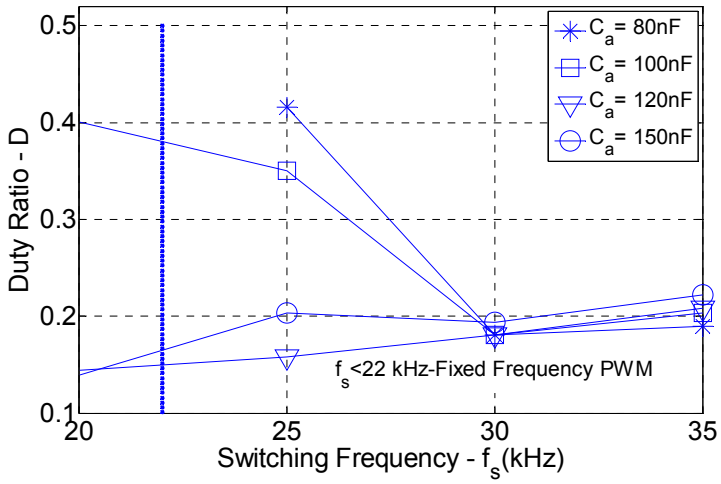
In Fig. 4.8(a), the ranges for C_a and f_s are 80 nF < C_a < 200 nF and 35 kHz < f_s < 55 kHz. When the curves in Fig. 4.8(a) are observed, it should be noted that not every curve stretches from 35 kHz < f_s <55 kHz and 0 < D < 0.5. This is because at least one of the design criteria mentioned in Section 3.5 cannot be achieved beyond the limits shown. If C_a and f_s are both too large voltage regulation will be correct; however, then there will not be sufficient t_{on} for C_a to fully discharge, which affects the input power factor. t_{on} (= D/f_s) has an upper limit due to D_{max} = 0.5 in the buck operation; thus, the larger the value of C_a is, the smaller the rate of change of voltage across it is so that the input capacitors are in DVM for only for a part of the input line cycle. For example, in Fig. 4.8(a), if C_a is increased beyond 200 nF and f_s = 55 kHz, then D must be increased beyond 0.5 in order



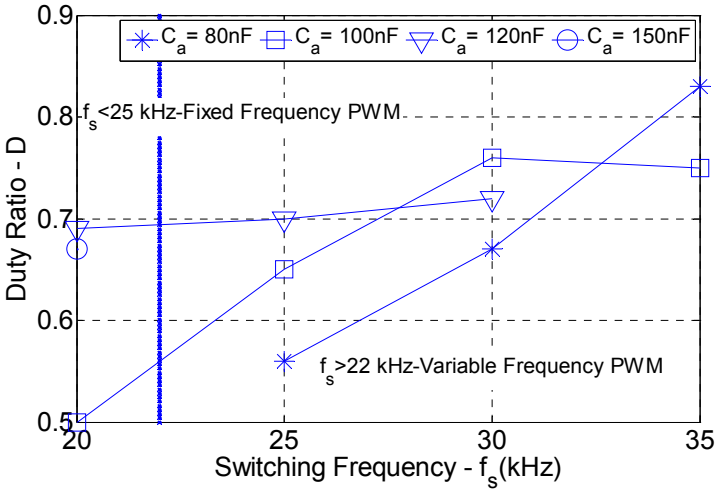
(a). Operating points for $M = V_o/V_{in} = 150/220\sqrt{2}$ & DVM [$V_o = 150$ V, $P_o = 2$kW].



(b). Operating points for $M = V_o/V_{in} = 150/220\sqrt{2}$ & DVM [$V_o = 500$ V, $P_o = 2$kW].



(c). Operating points for $M = 0.48$ and DVM [$V_o = 150$ V, $P_o = 500$W]



(d). Operating points for $M = 1.61$ & DVM [$V_o = 500$ V, $P_o = 500$W].

Fig 4.8: Input PFC and voltage gain - Design curves.

to for the input capacitors to be fully discontinuous, which is impossible for buck mode of operation. On the other hand, if both C_a and f_s are closer to their lower limits, then it is very difficult to obtain the required output voltage at steady-state (M will be smaller than required). This is because the smaller the value of C_a is, the less energy is stored in the input capacitors. Although the charging time can be increased by reducing D, this will affect the discharging of C_a and it will not fully discharge. For example, when $C_a = 80$ nF, f_s cannot be decreased below 45 kHz without decreasing the voltage gain (M).

Based on these factors for buck full load operation, D is set as 0.5 as it is the maximum limit for D and the converter will be able to operate with $D \leq 0.5$ for lighter loads. When Fig. 4.8(a) is observed, it can be seen that when $D = 0.5$ (or closer to 0.5), $C_a = 100$ nF and $f_s = 35$ kHz. For this iteration, if these values are selected then the next step is to find f_s and D value for other V_o/P_o combinations such that t_{on} is fixed. If this cannot be done, D must be changed and appropriate C_a and f_s must be found again. This is an iterative process and only the final iteration is shown here.

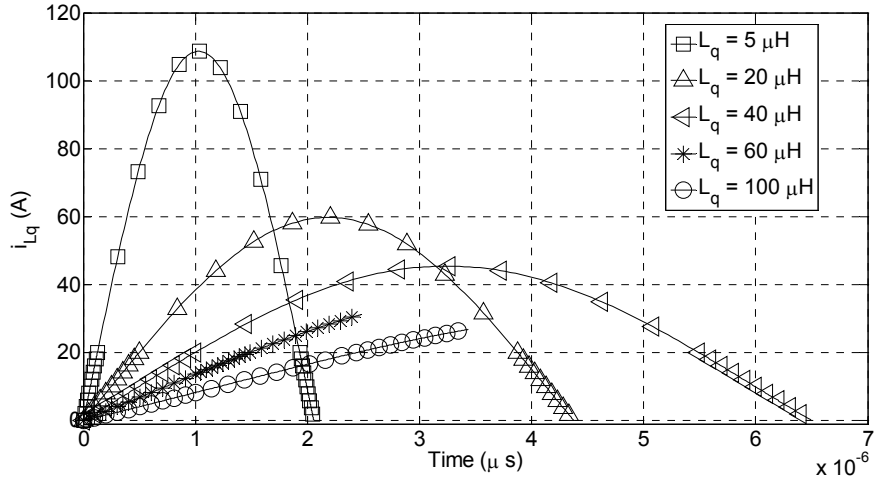
Step 2: Check selected C_a for other V_o/P_o combinations

Now that C_a is chosen for V_o = 150 V, P_o = 2 kW, the next step is to see if same C_a can be used for other V_o / P_o combinations such that t_{on} is constant as long as f_s > 22 kHz, above the audible range. If Fig. 4.8(b) is considered for V_o = 150 V, P_o = 2 kW, when C_a = 100 nF, f_s - D can have several combinations; however since f_s is above the audible range t_{on} must be approximately 14 µs. Therefore f_s = 40 kHz and D = 0.55 is selected for boost full load operation. Using Fig. 4.8(c), f_s and D can be found for buck light load operation so that t_{on} =14 µs, which results in f_s = 25 k Hz and D = 0.35.

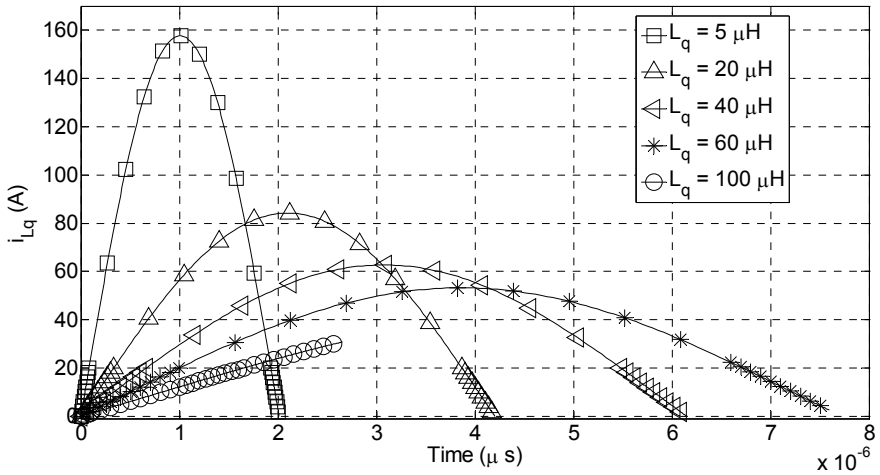
For boost light load operation, it is not possible to find a f_s-D combination for C_a = 100 nF beyond 22 kHz, such that t_{on} is a constant. The selected operating point is therefore f_s = 20 kHz and D = 0.5 and the controller changes from variable frequency control to fixed frequency PWM control.

B. Confirming the Quasi-resonant components (L_q and C_q)

After confirming the f_s-D combinations for the selected input capacitor, it is checked in this step if the chosen L_q and C_q components in the previous iteration still give the ZCS operation for both buck and boost modes under full load condition. It is assumed that the ZCS operation is obtained at light load conditions as the current is less. Fig. 4.9 shows the curves of i_{Lq} for different L_q values when C_a = 100 nF (selected above), C_q = 300 nF (previous iteration), t_{on} = D/f_s as calculated above. Fig. 4.9(a) is for buck full load operation and Fig. 4.9(b) is for boost full load operation. It can be seen higher the value of L_q, lower is the peak switch current and longer it will take current to become zero. Since the switch must be turned off after current becomes zero (ZCS operation) L_q and C_q must be changeable to the already selected C_a, f_s and D. If L_q = 40 µH then the peak current is around 60 A (boost operation) and current becomes zero during the switch on-time (t_{on}) for both buck and boost modes. Although L_q can be further increased to reduce the peak switch current, ZCS operation, especially in the buck mode can be affected, as shown in Fig. 4.9(a).



(a). Variation of i_{Lq} when L_q is changed (C_a = 100 nF, C_q = 300 nF, V_o=150V, P_o = 2 kW)



(b). Variation of i_{Lq} when L_q is changed (C_a = 100 nF, C_q = 300 nF, V_o = 150V, P_o = 2 kW)

Fig 4.9: ZCS operation – Design curves.

In a similar manner C_q can be changed by keeping L_q as its value in the previous iteration; however since the procedure is almost the same it is not shown here.

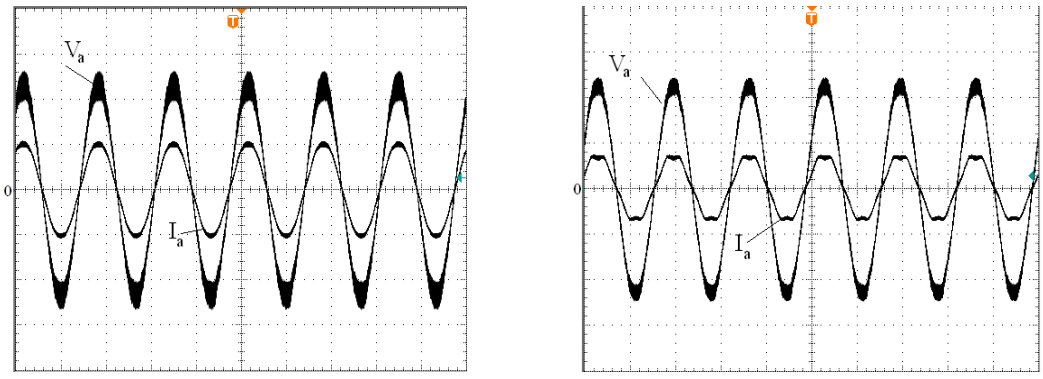
4.6 Experimental Results

To prove the concepts discussed in this chapter, a prototype of the proposed circuit was made using the following component values: Input inductors $L_a = L_b = L_c$ = 1 mH,

input capacitors $C_a = C_b = C_c = 100$ nF, resonant components $L_{q1} = L_{q2} = 40$ µH, $C_{q1} = C_{q2} = 300$ nF, output filter inductor $L_o = 1.3$ mH and output filter capacitor $C_o = 1500$ µF.

- Fig. 4.10 shows the input current and voltage for phase A when the converter is operating at full load with different output voltage values. Fig. 4.10(a) corresponds to buck mode of operation ($D < 0.5$) and Fig. 1(b) shows the same waveforms for boost mode of operation ($D > 0.5$). According to Figs. 4.10(a) and (b), the converter has a sinusoidal line current not only when $D < 0.5$ but also when $D > 0.5$.

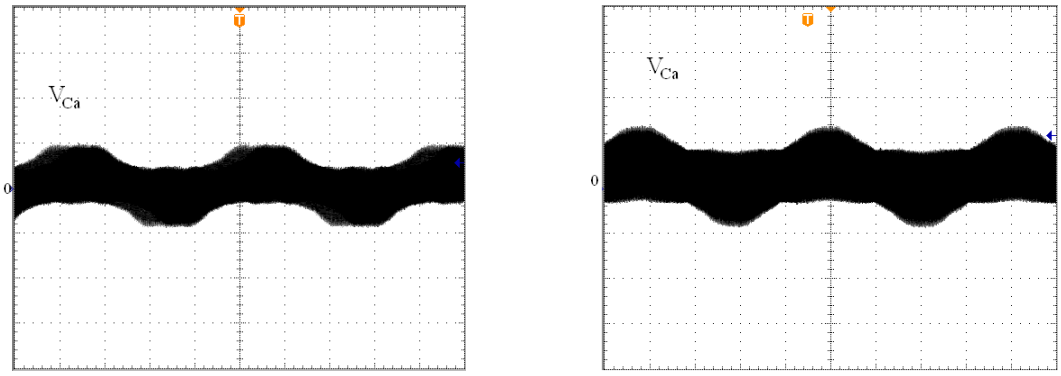
- Based on Fig. 4.10(b) it can be seen how the input PF is improved by the quasi-resonant buck-boost converter with respect to the fixed frequency buck-boost converter introduced in Chapter 3 (Fig. 3.14(b)).
- In order to get smooth sinusoidal line currents, the input filter capacitor voltages (V_{Ca}, V_{Cb} and V_{Cc}) must cross the zero axis as they are being discharged during each switching cycle, before they start to charge in the opposite direction. Fig. 4.11 shows the phase voltages across the input capacitor C_a for several line cycles and Fig. 4.12 shows V_{Ca} for several switching cycles that occur at the peak phase A voltage. Figs. 4.11(a) and 4.12(a) refer to buck mode of operation while Figs. 4.11(b) and 4.12(b) refer to boost mode of operation.



(a) (b)

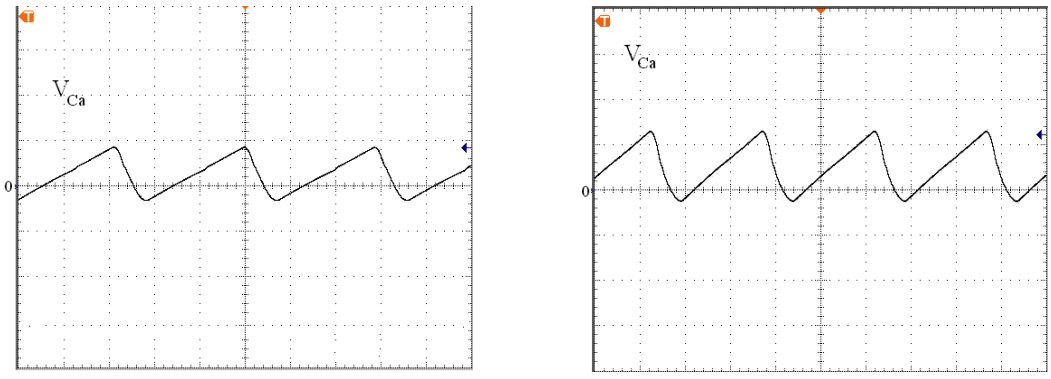
Fig 4.10: Phase voltage and line current $P_o = 2$ kW, $V_2 =$ (a) 150 V and (b) 500 V [V: 100 V/div, I: 10 A/div, t: 10 ms/div].

- When the switch S_1 is turned on, C_a discharges and becomes zero before it starts to charge in the opposite direction ($-V_{Ca}$). C_a begins to charge once S_1 is turned off. Similarly when S_2 is turned on, capacitors C_b and C_c begin to discharge; once S_2 is turned off C_b charges with I_b and C_c charges with I_c.
- The input capacitor C_a in the fixed frequency two-switch buck-converter (Fig. 3.1) discharges when S_1 is turned and V_{Ca} becomes zero and remain at zero until S_1 off. Unlike the buck-boost converter in Fig. 3.1, C_a in the quasi-resonant (QR) buck-boost converter does not stop at zero voltage instead charge in the opposite direction until the minimum voltage of C_a, $V_{Ca,min} = -V_o$ because C_a is connected across the load by the neutral point connection and the output diodes. This change,



(a) (b)

Fig 4.11: Input capacitor phase voltage for line cycles $P_o = 2$ kW, $V_2 =$ (a) 150 V and (b) 500 V [V: 1000 V/div, t: 4 ms/div].



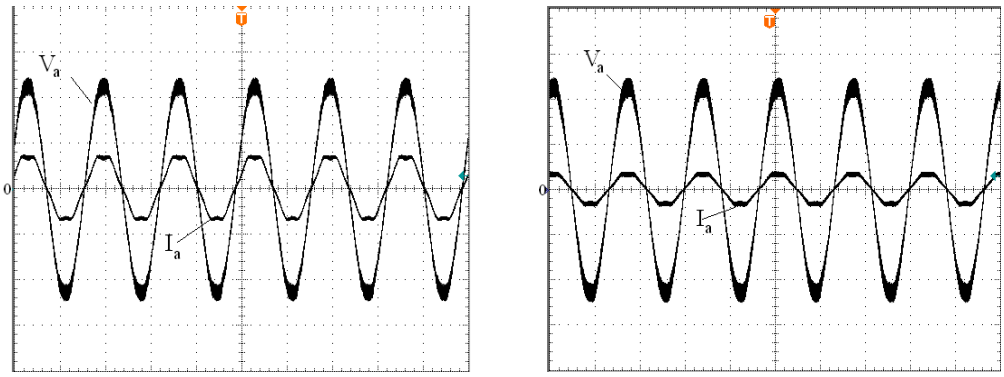
(a) (b)

Fig 4.12: Input capacitor phase voltage for line cycles $P_o = 2$ kW and $V_2 =$ (a) 150 V, (b) 500 V [V: 750 V/div, t: 10 µs/div].

however, does not affect the sinusoidal envelope of average V_{Ca} and therefore does not affect the input power factor.

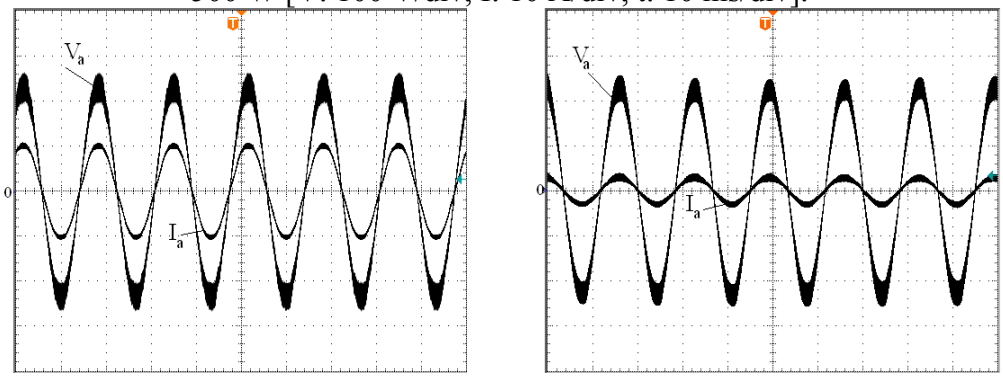
- For $D < 0.5$, the effect of output load on the line current is illustrated in Fig. 4.13. Fig. 4.13(a) shows the line current and phase voltage for P_o = 2 kW and Fig. 4.13(b) shows the same for P_o = 500 W. It can be seen that the line current is nearly sinusoidal at all loads. This is only possible due to the QR variable frequency nature of the converter as the input capacitors are forced to discharge by the high DC side currents.
- For $D > 0.5$, the impact of output load on the line current is illustrated in Fig. 4.14. Fig. 4.14 shows the line current and phase voltage for output power at (a) 2 kW and (b) 500 W. It can be seen unlike for the fixed frequency buck-boost front-end converter the proposed converter has excellent input PFC even at boost mode.
- The harmonics content of the input line current in rms values is given in Table 4.1 together with the input power factor. Table 4.1 also indicates the IEC 61000-3-2 Class A standard limits for maximum allowable harmonics to the utility.
- Fig. 4.15 shows the switch voltage (V_S) and current (I_S) for one of the IGBTs for different output conditions. V_S has a triangular shape and its peak equals the peak of V_{Ca}. I_S is the sum of the line current (I_a) and the discharging current of C_a and has a resonant shape. I_S becomes zero due to resonance between L_q and C_q before the switch is turned off hence ZCS operation is achieved.

Efficiency measurements of the QR buck-boost converter were made and were compared to those of the buck-boost converter presented in the previous chapter. It was found that the QR buck-boost converter was less efficient than the hard-switched buck-boost converter even though it has fewer switching losses. This is because of the presence of circulating current that is due to the resonant nature of the converter that the buck-boost converter presented in Chapter 3 does not have. This finding is consistent with what has been reported in the literature where it has been shown that resonant converter are to be preferred over hard-switching converters for higher power application such as 6 kW [44]. The maximum load of 2 kW was the maximum load that was available so that



(a) (b)

Fig 4.13: Input current and voltage when V_o = 150 V and P_o = (a) 2 kW and (b) 500 W [V: 100 V/div, I: 10 A/div, t: 10 ms/div].



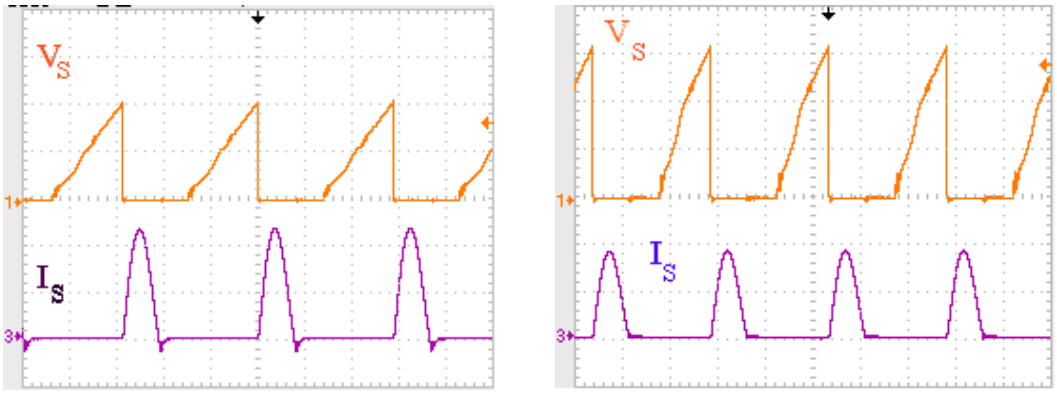
(c) (d)

Fig 4.14: Input current and voltage when V_o = 500 V and P_o = (a) 2 kW and (b) 500 W [V: 100 V/div, I: 10 A/div, t: 10 ms/div].

Table 4.1 IEC 61000–3–2 Class A standard limits, harmonics of phase current efficiency values V_o/P_o combinations.

Harmonics	Class A	150 V/2kW	150 V/500W	500V/2 kW	500 V/500 W
5^{th}	2.06	0.1357	0.0582	0.1098	0.0059
7^{th}	1.39	0.0156	0.0174	0.052	0.0038
11^{th}	0.6	0.0163	0.0099	0.0125	0.0006
13^{th}	0.38	0.00099	0	0.0126	0
PF		0.9976	0.998	0.9993	0.9977

efficiency measurements could not be made with heavier loads, in the load range where the superiority of resonant converters has been established.



(a). [I: 25 A/div, t: 10 µs/div] (b). [I: 30 A/div, t: 10 µs/div]

Fig 4.15: Switch voltage (V_S) and Current (I_S) for P_o = 2 kW (a) V_2 = 150 V and (b) V_o = 500 V [V: 100 V/div].

4.7 Conclusion

In this chapter, a new three-phase AC-DC, two-switch, neutral point connected multilevel buck-boost converter was proposed as a front-end converter in a two-stage AC-DC converter. This new reduced-switch AC-DC front-end converter is a quasi-resonant resonant converter - its switch currents are shaped by resonant circuit elements so that they fall to zero before the switches are turned off, thus reducing switching losses.

Due to its quasi-resonant nature and its operation with variable frequency control, the proposed converter can have near-sinusoidal input currents for both buck and boost modes and also at very light load conditions. This is in contrast to the previous hard-switched buck-boost converter, which had difficulty getting sinusoidal input currents in the boost mode and at light load conditions.

In this chapter, the basic principles of variable switching frequency and quasi-resonance are explained, the steady-state operation of the proposed converter were detailed, its steady-state characteristics are determined by analysis and are then presented for both stepping up (boost mode) and down (buck mode) of input voltage. Based on the results of the analysis, a procedure that can be used in the design of the converter's key

components was developed and then demonstrated with an example. The feasibility was confirmed with results obtained from an experimental prototype.

Chapter 5

5 A Three-Phase Single-Stage AC-DC PWM Buck-Type Full-Bridge Converter

5.1 Introduction

Chapters 2 – 4 of this thesis have thus far explored new reduced switch AC-DC front-end converters to reduce the number of switching devices that are found in conventional two-stage AC-DC converters. These new front-end converters are based on three-phase single-switch converters and have multilevel structures that reduce the peak voltage stress of their switches. In Chapter 2, the synthesis of multilevel topologies from single-switch topologies are discussed and a new family of neutral-point connected reduced switch multilevel converters was introduced. One converter from this family, the buck-boost converter, was further examined in Chapter 3 and the use of quasi-resonance to reduce switching losses was examined in Chapter 4. The proposed reduced switch front-end converters can be used for as an alternative to the six switch front-end converter of a two-stage converter.

Reducing the number of switches in the front-end AC-DC converter of a two-stage AC-DC converter is only one way to reduce its overall switch count – thus simplifying the converter topology and reducing its cost. Another way is to combine the front-end AC-DC converter and the back-end DC-DC converter into a single converter, a discussed in Section 1.3 of this thesis. Doing so results in converters that are even simpler and less expensive than two-stage converters with reduced switch front-end converters, given that they only have one converter stage that simultaneously performs both input power factor correction (PFC) and DC-DC conversion (converting the intermediate DC-DC bus voltage into the desired out DC voltage). Single-stage converters are the preferred choice for low cost high power applications. However due to the fact that intermediary DC voltage is not regulated like in two-stage PFC; single-stage will suffer from lower efficiency.

Most previously proposed three-phase single-stage converters [16]-[23] have a boost converter input section and thus have several drawbacks including high input ripple as their input currents are discontinuous with high current peaks, high output ripple due to a lack of an output inductor. Moreover, converters of this type that lack a bulk capacitor at the primary-side DC bus have a large low frequency 360 Hz component at the output, which limits their application. Converters that do have this bulk capacitor do not have this particular drawback, but their DC bus voltage may become excessive, particularly at light loads.

Although work has been done on boost-based, three-phase AC-DC, single-stage full-bridge converters, little, if any, work has been done on buck-based three-phase AC-DC single-stage full-bridge converters. These are converters that are based on the combination of a buck front-end converter and a DC-DC converter instead of a boost front-end converter. Such buck-based converters do not have the drawbacks of boost-based single-stage converters such as high input current and output current ripple. Their true potential, however, is uncertain as their properties and characteristics have not been thoroughly examined.

In this chapter, a new AC-DC single-stage PWM full-bridge converter is proposed. The steady-state operation of the converter is explained and the modes that the converter goes through during a half switching cycle are shown. The steady-state characteristics of the converter are determined by mathematical analysis and are used to develop a procedure for the design of key converter components. The feasibility of the new converter is confirmed with results that were obtained from an experimental prototype.

5.2 A Three-Phase Single-Stage AC-DC PWM Buck-Type Full-Bridge Converter

The buck-based converter that is examined in this chapter is shown in Fig. 5.1. It has three sections: an input section that consists of a three-phase diode bridge rectifier with a three-phase L-C filter; a DC bus section that consists of an inductor (L_{bus}), a capacitor (C_{bus}) and two diodes (D_{bus1} and D_{bus2}); and a full-bridge converter section.

The proposed converter is essentially an isolated buck converter as it steps downs the input voltage and has transformer isolation. The converter in Fig. 5.2(a) achieves PFC by making the input capacitors charge and discharge during every switching cycle; so that the voltages across the input capacitors look as the waveform in Fig. 5.2(b) - a triangle train of pulses that is bounded by a sinusoidal envelope so that it is essentially sinusoidal with high-frequency harmonics. The following should be noted about the general operation of the proposed converter:

- As explained in Section 1.2.1 of this thesis, a DC-DC full-bridge converter alternates between freewheeling modes (S_1 and S_3 or S_2 and S_4) and power-transfer modes (S_1 and S_2 or S_3 and S_4). This is analogous to the turning off and on of the front-end buck switch (S_b) in Fig. 5.2(a). The input capacitors charge during the freewheeling modes of the full-bridge section when two top switches or two bottom switches are on, and discharge during power-transfer modes of operation when a diagonally opposed pair of switches are on and power can be transferred from the input to the output. The PFC occurs naturally, without the need for any input section sensing, as long as the input capacitor voltages are discontinuous in all the switching cycles contained in an input line cycle.
- The converter shown in Fig. 5.1 has been synthesized using quadratic converter circuit theory, as shown in [45]. It is possible to take two cascaded DC-DC buck converters and convert them into a single so-called quadratic DC-DC converter (called quadratic because its output to input ratio is dependent on the square of the

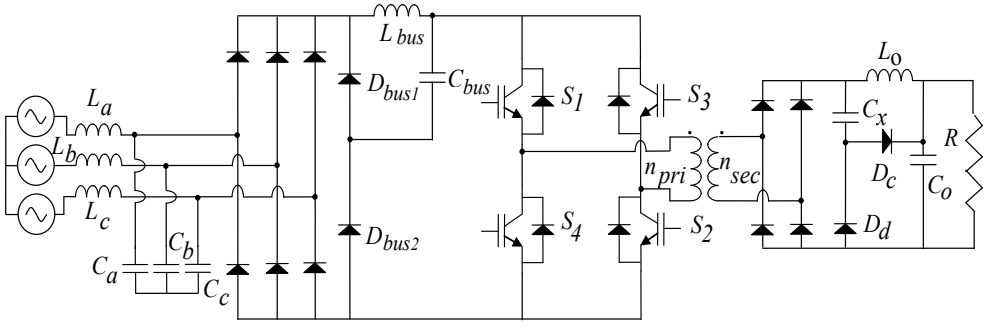
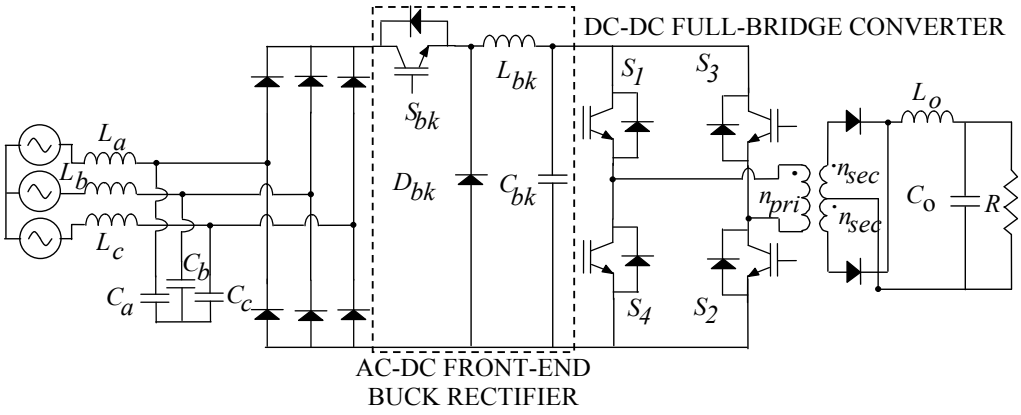
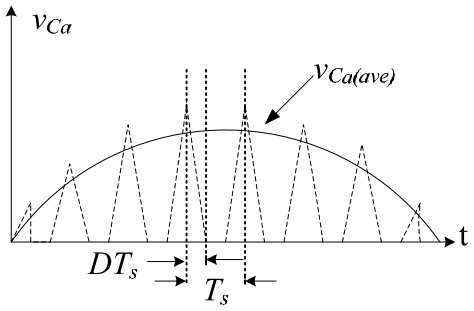


Fig 5.1: Three-phase single-stage buck-type full-bridge converter.



(a). AC-DC single-switch buck rectifier and DC-DC full-bridge converter.



(b). Input capacitor phase voltage.

Fig 5.2: AC-DC single-switch buck rectifier and DC-DC full-bridge converter

converter's duty cycle D^2 instead of just D). The topology shown in Fig. 5.1 can be derived in a similar manner except that the input DC source is replaced by a three-phase AC source and diode bridge and the second cascaded converter is a full-bridge converter (isolated buck converter) instead of a buck converter.

- Capacitor C_{bus} must be disconnected from the rest of the converter when the full-bridge is in a freewheeling mode of operation because the input capacitors would not be allowed to charge properly otherwise. The improper charging of these capacitors would result in their voltages not being bounded by a sinusoidal envelope, which would ultimately lead to distortion in the input currents and a lower input power factor.

- The fact that C_{bus} is disconnected from the converter by the reverse-blocking of diode D_{bus2} when the converter is in a freewheeling mode does not affect the

operation of the full-bridge as it operates like a PWM full-bridge converter in freewheeling mode. Nor does this fact affect the operation of the full-bridge when it is in an energy-transfer mode as C_{bus} is connected to the DC bus during such a mode because D_{bus2} is forward-biased. In other words, the full-bridge can therefore operate exactly like a PWM DC-DC full-bridge converter.

- Since C_{bus} is disconnected from the new converter whenever a freewheeling mode occurs, it is therefore not in the circuit when the full-bridge is exiting a freewheeling mode. As a result, there is no path for any reverse current from the full-bridge to flow in the DC bus and some steps must be taken to address this problem.
- As a means to simplify the analysis of the converter and to discover the characteristics of the new fundamental buck-based converter, any reverse current from the full-bridge is absorbed by using dissipative snubbers. Doing so, however, results in the converter performance being less than optimal (especially efficiency), as will be discussed towards the end of this chapter.
- The converter operation is, however, considered with some zero-voltage-zero-current switching (ZVZCS) method. It is a means to improve converter efficiency without interfering with the basic operation of the converter [46]-[51].

5.3 Operation of the Proposed Converter

The most significant modes of operation that the converter goes through during a half switching cycle are presented in this section. The equivalent circuit diagrams and typical converter waveforms that show these modes of operation are given in Figs. 5.3 and 5.4 respectively.

In Fig. 5.3, only the components that are conducting in a particular mode are shown, with the output capacitor and load shown as an equivalent voltage source V_o and the transformer magnetizing current neglected. The input voltage source over an interval of 60º of the fundamental period is considered here. An interval of 60º of the fundamental period is used due to symmetries in the rectified diode bridge output waveform.

It should be noted that any interval of 60º of the fundamental period can be considered for the analysis. For this case an interval of 60º of the line cycle when the phase A input voltage is positive and the phase B and C voltages and are both negative is considered. One full-switching cycle of the full-bridge section of the converter consists of two input section half-switching cycles, as there are two energy-transfer modes and two freewheeling modes in a full-bridge switching cycle. As a result, a full-bridge half-switching cycle k in a 60º interval of the fundamental period is considered below, to explain the converter operation, the modal equations and the converter analysis.

Mode 0 ($t < t_0$), [Fig. 5.3(a]:

Mode 0 refers to the initial conditions. Before $t = t_0$, The secondary side auxiliary capacitor C_x is fully discharged ($V_{Cx,k(t0)} = 0$) and the initial transformer current is negligible ($I_{Llk,k(t0)} = 0$). Current in the DC bus is flowing through diode D_{bus1}, inductor L_{bus}, and capacitor C_{bus}. Diode D_{bus2} is off because it is reverse biased by $v_{rec,k}$ as D_{bus1}, is conducting. The input capacitors are charging with the line currents and will reach the peak voltages, which are directly related to the line currents for a full-bridge half-switching cycle k.

At $t = t_0$, the instantaneous voltage of C_a for the k^{th} full-bridge half-switching cycle ($v_{Ca,k}$) is the voltage at the end of the $(k - 1)^{th}$ full-bridge half-switching cycle and is the peak voltage. If $I_{a,k-1}$ was the phase A line current and $V_{Ca,k-1(pk)}$ was the peak voltage of C_a for the $(k - 1)^{th}$ full-bridge half-switching cycle, then voltage of C_a at $t = t_0$, ($V_{Ca,k(t0)}$) can be expressed as

$$V_{Ca,k(t0)} = V_{Ca,k-1(pk)} = \frac{I_{a,k-1}}{C_a}(1-D)\frac{T_s}{2} \tag{5.1}$$

where D is the duty ratio and is the amount of time that a pair of diagonally opposed switches is on with respect to the half-switching cycle period ($D = t_{on,pair}/(T_s/2)$), T_s is the switching period and C_a is the input capacitance. The resulting three-phase diode bridge rectifier output voltage, $v_{rec,k(t0)}$ can be calculated using the line-line voltage of C_a as

$$V_{rec,k(t0)} = \sqrt{3}V_{Ca,k(t0)} = \sqrt{3}\frac{I_{a,k-1}}{C_a}(1-D)\frac{T_s}{2} \tag{5.2}$$

The initial L_{bus} current can be taken as the average of $i_{Lbus,k}$ for k^{th} half-switching cycle

$$I_{Lbus,k(t0)} = I_{Lbus,k(ave)} = D\frac{I_o}{n} \tag{5.3}$$

where I_o is the DC load current, and the initial voltage of C_{bus} can be taken as the average voltage of C_{bus} because the instantaneous voltage can assumed to be constant given that C_{bus} is a bulk capacitor

$$V_{Cbus} = \frac{nV_o}{D} \tag{5.4}$$

where n is the turns ratio and V_o is the output DC voltage. The modal equations for k^{th} full-bridge half-switching cycle are given below, based on the initial conditions mentioned above.

Mode 1 ($t_o < t < t_1$), [Fig. 5.3(b)] :

At $t = t_0$, switch S_2 is turned on and current starts to flow into the full-bridge from the DC bus. L_{bus} is charging and its current $i_{Lbus,k}$ is made up of line current $I_{a,k}$ and the discharging current ($i_{Ca,k}$) of C_a. Since diagonally opposite switches S_1 and S_2 are on, the voltage across C_{bus} (V_{Cbus}) is applied across the transformer primary and power is transmitted to the load from the input side. The primary current, $i_{Llk,k}$ increases and once it equals the reflected load current L_{lk} starts to resonate with C_x so that C_x begins to be charged. This resonant current ($i_{Llk,k}$) is reflected to the secondary side of the transformer and feeds the load while charging C_x through the auxiliary circuit diode D_c. During this mode $i_{Llk,k}$ reaches its peak value due to resonance and C_x reaches its peak voltage at the end of Mode 1. $i_{Llk,k}$ at $t = t_1$ equals the reflected load current (= I_o/n). C_a discharges as follows:

$$i_{Ca,k}(t) = -C_a\frac{dv_{Ca,k}}{dt} \tag{5.5}$$

where $i_{Ca,k}$ is the discharging current of C_a. $i_{Ca,k}$ can be stated as

$$i_{Ca,k}(t) = i_{Lbus,k} - I_{a,k} \tag{5.6}$$

Eq. (5) can be rewritten using Eq. (6) to obtain $dv_{Ca,k}/dt$

$$\frac{dv_{Ca,k}}{dt} = -\frac{1}{C_a}(i_{Lbus,k} - I_{a,k}) \tag{5.7}$$

Eqs. (8) and (9) define the behavior of the DC bus components in Mode 1

$$v_{Lbus,k}(t) = L_{bus}\frac{di_{Lbus,k}}{dt} \tag{5.8}$$

$$\frac{dV_{Cbus}}{dt} = 0 \tag{5.9}$$

where $v_{Lbus,k}$ is the instantaneous voltages of L_{bus} and V_{Cbus} is a constant. $v_{Lbus,k}$ is the difference between $v_{rec,k}$ and V_{Cbus}; hence Eq. (8) can be rewritten as

$$\frac{di_{Lbus,k}}{dt} = \frac{v_{rec,k} - V_{Cbus}}{L_{bus}} \tag{5.10}$$

V_{Cbus} is applied across L_{lk} and the transformer primary winding. The transformer secondary voltage equals the sum of $v_{Cx,k}$ and V_o. Eq. (11) gives d$i_{Llk,k}/dt$ in Mode 1

$$\frac{di_{Llk,k}}{dt} = \frac{v_{Llk,k}}{L_{lk}} = \frac{V_{Cbus} - n(V_o + v_{Cx,k})}{L_{lk}} \tag{5.11}$$

Eq. (12) shows the rate of charging of C_x during Mode 1 based on the resonance of L_{lk} and C_x

$$\frac{dv_{Cx,k}}{dt} = \frac{ni_{Llk,k} - I_o}{C_x} \tag{5.12}$$

Mode 2 ($t_1 < t < t_2$), [Fig. 5.3(c)] :

At $t = t_1$, C_x reaches its peak voltage and stops being charged. The input capacitors continue to discharge into the full-bridge. $v_{Ca,k}$ continues to decrease. The voltage of C_{bus} is applied across the primary winding and $i_{Llk,k}$ equals the reflected I_o during Mode 2 because C_x and L_{lk} no longer resonates. Therefore, the same modal equations for Mode 1 [Eqs. (5) - (10)] are valid for Mode 2 as well, but with the conditions of

$$dv_{Cx,k}/dt = 0, di_{Llk,k}/dt = 0 \tag{5.13}$$

The simplification results in

$$i_{Lbus,k}(t) = I_{a,k} + cos\left(B_1(t-t_1)\right)\left(I_{Lbus,k(t1)} - I_{a,k}\right) + \left(\sqrt{3}V_{Ca,k(t1)} - V_{Cbus}\right)\left(\sqrt{C_a/L_{bus}}\right)sin\left(B_1(t-t_1)\right) \tag{5.14}$$

where $B_1 = \sqrt{\sqrt{3}/C_a L_{bus}}$ and

$$v_{Ca,k}(t) = \frac{L_{bus}}{\sqrt{3}}\frac{di_{Lbus,k}}{dt} + V_{Cbus} \tag{5.15}$$

Mode 3 ($t_2 < t < t_3$), [Fig. 5.3(d)] :

The input capacitors should be sufficiently small so they can discharge before the converter changes from a power transfer mode to a freewheeling mode. At $t = t_2$ these capacitors discharge fully and thereafter remain discharged until a short-circuit mode of the full-bridge starts. Once the input capacitors are discharged the line currents (e.g. $I_{a,k}$) from the grid side continue to flow into the DC side instead of flowing in to the input capacitors. $I_{a,k}$ flows into the DC side until S_1 is turned off because $I_{a,k}$ can no longer flow through the three-phase diode rectifier into the DC side.

Since the input capacitors have no voltage across them during this mode $v_{rec,k}$ is also zero. When $v_{rec,k}$ becomes zero, D_{bus1} and D_{bus2} in the DC bus section become forward biased and conduct current. L_{bus} discharges into C_{bus} through D_{bus1}, and C_{bus} continues to

discharge into the full-bridge though D_{bus2} so that V_{Cbus} is still applied across the transformer primary. The voltage across L_{bus} equals the negative of $v_{rec,k}$ until the next power transfer mode starts at $t = T_s/2$. The current in the transformer and the voltage of C_x are same as in Mode 2.

$$v_{Lbus,k}(t) = -V_{Cbus} \tag{5.16}$$

Mode 4 ($t_3 < t < T_s/2$), [Fig. 5.3(e)] :

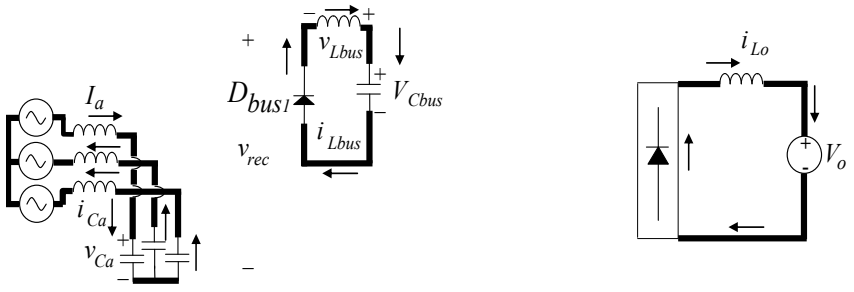
At $t = t_3$, switch S_1 is turned off and the body diode of S_4 starts to conduct the negative switch current of S_4 until it **is** turned on; the same happens to S_1 and it conducts negative current in the other half-switching cycle. The converter enters a freewheeling mode at the start of this mode. The connection between the AC side and the DC side is broken so that the entire line currents (e.g. $I_{a,k}$) flow through the input capacitors (e.g. C_a) and they begin to charge, according to

$$v_{Ca,k}(t) = \frac{I_{a,k}}{C_a}(t - t_3) \tag{5.17}$$

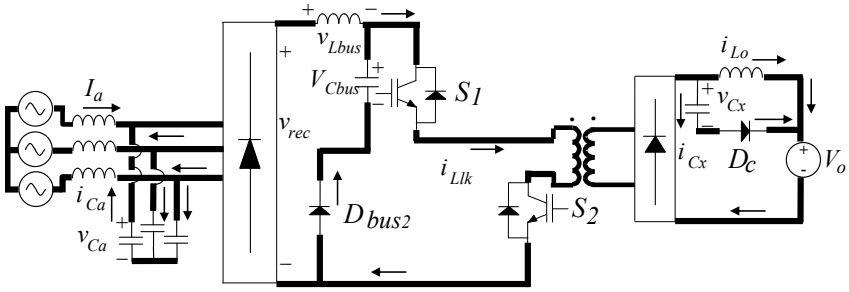
When $v_{Ca,k}$ increases, so does $v_{rec,k}$ and, as a result, the voltage stress of the switches that are off during this mode also increase (e.g. $v_{S1,k}$). C_x begins to discharge at the start of this mode.

Current $i_{Lbus,k}$ freewheels through L_{bus}, C_{bus}, and D_{bus1} and no current enters the full-bridge during this mode because D_{bus2} is reversed biased by $v_{rec,k}$. $i_{Llk,k}$ freewheels through S_4, S_2 and the primary winding. During Mode 4, the full-bridge is in a freewheeling mode, but a counter voltage is impressed across L_{lk} due to the presence of C_x on the transformer secondary side.

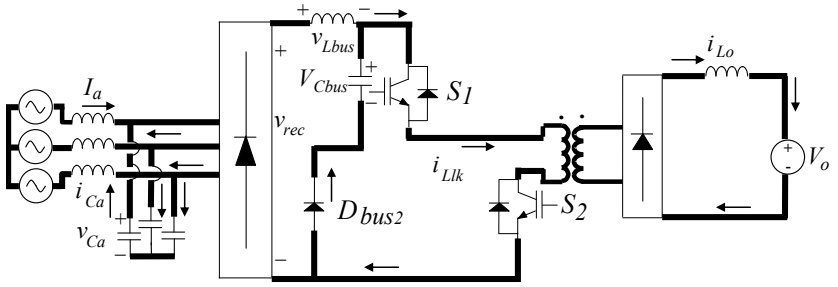
$v_{Cx,k}$ keeps the secondary side rectifier voltage above zero and impresses voltages across the transformer's secondary and primary windings. This causes a counter voltage and it decreases $i_{Llk,k}$. As a result, the secondary current also falls below I_o. In order to keep I_o constant, C_x discharges though D_d into L_o. Towards the end of Mode 4, the primary current is completely extinguished by the auxiliary capacitor C_x as given below



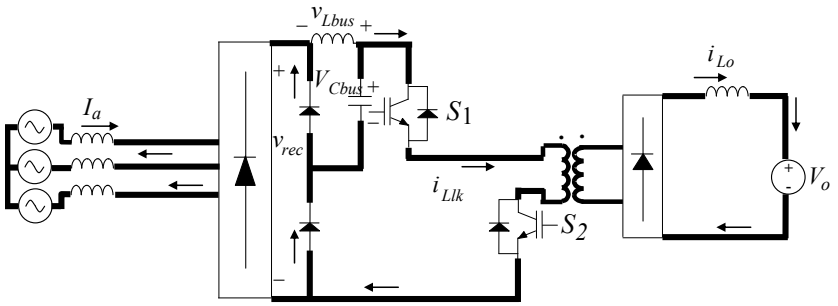
(a) Mode 0 [$t < t_0$]



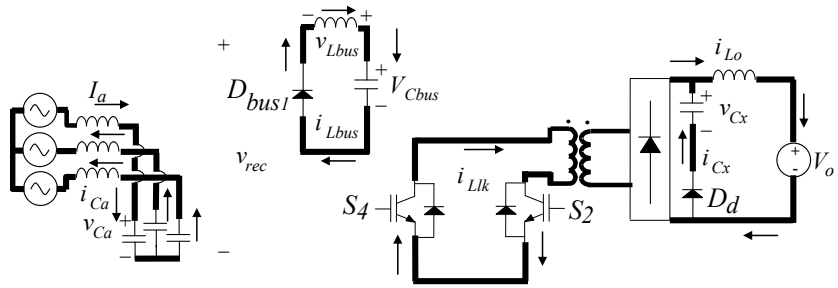
(b) Mode 1 [$t_0 < t < t_1$]



(c) Mode 2 [$t_1 < t < t_2$]



(d) Mode 3 [$t_2 < t < t_3$]



(e) Mode 4 [$t_3 < t < T_s/2$]

Fig 5.3: Modes of steady-state operation.

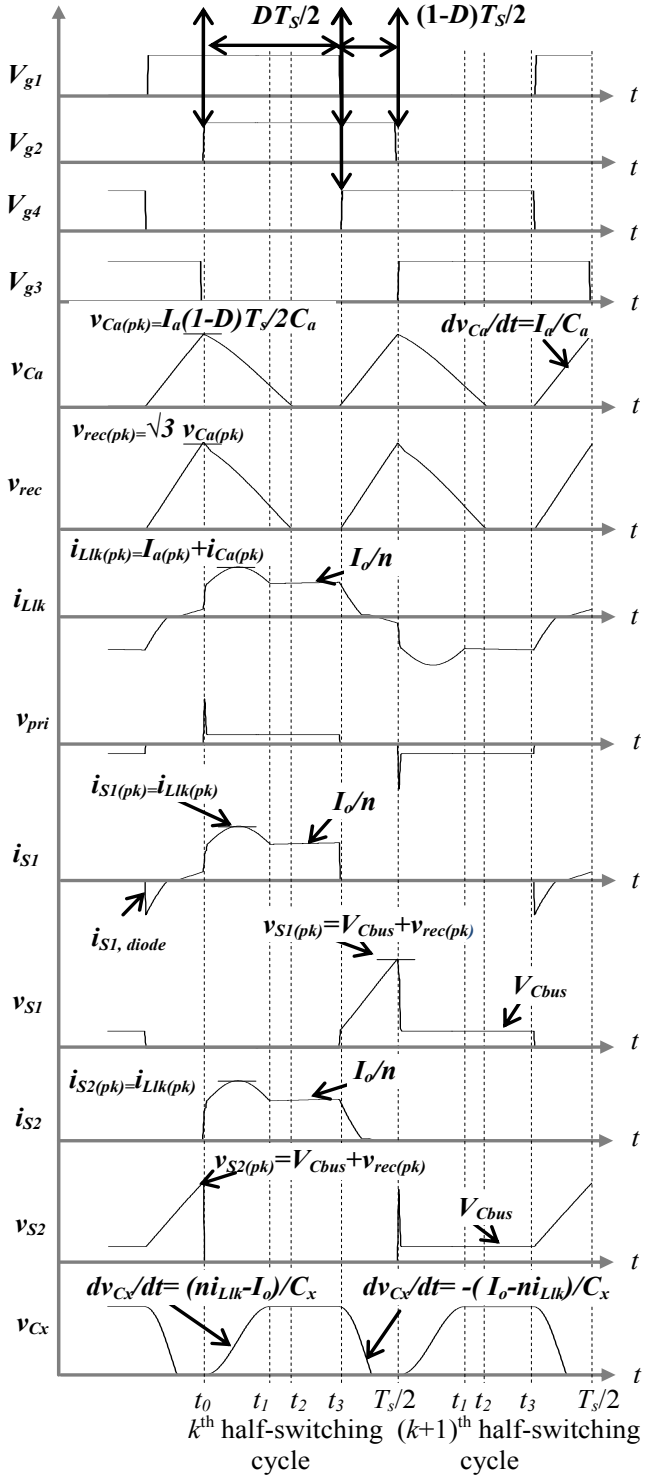


Fig 5.4: Typical waveforms of the converter under study.

$$\frac{d(i_{Llk,k})}{dt} = \frac{-nv_{Cx,k}}{L_{lk}} \tag{5.18}$$

where C_x discharges by giving the difference current (I_o - $ni_{Llk,k}$)

$$\frac{dv_{Cx,k}}{dt} = \frac{-\left(I_o - ni_{Llk,k}\right)}{C_x} \tag{5.19}$$

It should be noted that C_x discharges completely some time during this mode.

After $i_{Llk,k}$ becomes zero S_2 is turned off and switch S_3 is turned on at $t = T_s/2$ with very little current through it, as current through L_{lk} cannot change suddenly. With the turning on of S_3 input capacitors stop charging. Using Eq. (20) the peak input capacitor voltage for the k^{th} full-bridge half-switching cycle can be found

$$V_{Ca,k(pk)} = V_{Ca,k(Ts/2)} = \frac{C_a}{I_{a,k}}(1-D)\frac{T_s}{2} \tag{5.20}$$

This is the beginning of the $(k + 1)^{th}$ half of the switching cycle and the converter enters Mode 1, but with S_4 and S_3 on instead of S_1 and S_2. It should be noted that the peak switch voltage of S_2, $V_{S2,k(pk)}$ can rise to ($V_{rec,k(pk)} + V_{Cbus}$) after S_2 is turned off but before S_3 is turned on. $v_{S2,k(pk)}$ falls to the V_{Cbus} after S_3 is on. It should also be noted that the duration of this mode is $T_s/2 - t_3 = DT_s/2$.

5.4 Converter Analysis

In order to develop a solid understanding of the new converter's properties and characteristics and to develop a procedure that can be used to design the new converter, the steady-state behavior of the converter must be analyzed to determine its characteristic curves for any given set of specifications (line-to-line input voltage $V_{ll(rms)}$, output voltage V_o, output current I_o, and switching frequency f_s) and any given set of component values (input capacitors $C_a = C_b = C_c$, input inductors $L_a = L_b = L_c$, DC bus inductor L_{bus}, DC-bus capacitor C_{bus}, duty ratio D, transformer turns ratio $n = n_{pri}/n_{sec}$ and output inductor L_o).

After the key converter characteristics are determined, a design procedure can then be developed. The key parameters that need to be determined for the design of the converter are the voltage of C_{bus} (V_{Cbus}), the maximum input capacitor voltage $V_{Ca(pk)}$ (which will aid in finding the maximum switch voltage $v_{S(pk)}$), and the time $v_{Ca,k}$ takes to become zero in Mode 2 (which indicates whether the selected capacitor value will result a discontinuous or continuous $v_{Ca,k}$).

Given the interdependency of the components and key variables such as input capacitor voltage v_{Ca}, bus capacitor voltage V_{Cbus} etc. the analysis of the converter cannot be performed using equations with closed form solutions and some sort of a computer program must be used to solve the aforementioned modal equations. There are many ways to write such a program; one way of doing so is shown here.

The ultimate objective of the analysis is to find steady-state operating points. When the converter is in steady-state, the average voltage across an inductor or average current through a capacitor must be zero. For this analysis, the status of the converter is checked by evaluating the average value of the L_{bus} voltage, $V_{Lbus(ave)}$, over a period of one-sixth of a 60 Hz line cycle. If $V_{Lbus(ave)}$ is zero for this period, then the converter is in steady-state and a steady-state operating point has been determined.

In order to determine $V_{Lbus(ave)}$, there must be a process to find $v_{Lbus,k}$ for each switching interval, then consider the overall v_{Lbus} waveform over a period of one-sixth of a 60 Hz line cycle to find its average value. The $v_{Lbus,k}$ waveform during any k full-bridge half switching cycle can be found by using the appropriate modal equations derived in the previous section to calculate the voltage across the three-phase diode bridge rectifier ($v_{rec,k}$) and the voltage across capacitor V_{Cbus}, as $v_{Lbus,k}$ is the difference between $v_{rec,k}$ and V_{Cbus}. In order to calculate $v_{rec,k}$, the phase voltage of the input capacitors must be obtained (e.g. $v_{Ca,k}$). These input capacitor phase voltages are made up of trains of triangle pulses, where the triangle pulses consist of decreasing portions from t_0-t_2, zero portions from t_2-t_3 and rising portions from t_3 - $T_s/2$ for any full-bridge half-switching cycle k. The charging of a capacitor can be determined by Eq. (5.17), but determining the discharging is not straightforward. In order to find the discharging of the input capacitors,

the current $i_{Lbus,k}$ from t_0-t_2 must be obtained (Eq. (5.7)). Since C_{bus} is a bulk capacitor, the voltage ripple of V_{Cbus} can be neglected.

The following assumptions have been made to simplify the analysis:

- The input line currents (e.g. $I_{a,k}$) and source voltages can be considered to be constant during any switching cycle as the switching period T_s (= $1/f_s$) is much smaller than the line period T_l (= $1/f_l$).

- The low 360 Hz frequency ripple that exists in the C_{bus} voltage can be neglected so that V_{Cbus} is constant.

- The input line currents coming out of the source can be assumed to be sinusoidal with no ripple.

- L_o is sufficiently large so that the output current is ripple free; therefore, the average current of output filter inductor (L_o) equals I_o.

- Converter operation during dead times is ignored as the length of dead times is considered negligible in comparison with the rest of the switching cycle.

- The effects of the auxiliary circuit and the leakage inductance of the transformer can be neglected until after a range of valid steady-state operating points has been determined.

The analysis of the DC-DC full-bridge section of the converter can be performed once a set of component values for the input section, the transformer turns ratio, duty ratio and the output inductor has been chosen. Since this analysis is very similar to that of a ZVZCS-PWM DC-DC full-bridge converter [46], it will not be presented here.

A computer program can be implemented to perform the following steps to find a valid operating point and the equations that were derived in Section 5.3 of this chapter can be used as part of the program. The program could have the following steps:

- ***Step 0:*** Select the set of specifications and components values to be considered. To start the process, choose any value of D.
- ***Step 1:*** The input line current for the k^{th} full-bridge half-switching cycle is required to find the rising of input capacitor phase voltages as indicated in Eq. (5.17); therefore the calculation of $I_{a,k}$, is given here and the line currents can be determined in a similar manner.

$$I_{a,k} = I_{a(pk)} \sin\left(2\pi f_s t + \frac{\pi}{2}\right) \tag{5.21}$$

where $I_{a(pk)}$ is the peak phase A current and is calculated below

$$I_{a(pk)} = \sqrt{2}\,\frac{(V_o I_o)}{\sqrt{3} V_{ll(rms)}} \tag{5.22}$$

- ***Step 2:*** The value of V_{Cbus} can be approximated by Eq. (5.23) below, based on assumptions as

$$V_{Cbus} = \frac{nV_o}{D} \tag{5.23}$$

Once V_{Cbus} is calculated it is important to verify that $i_{Lo,k}$ is actually continuous. This can be done by using the following equation to see if the average current component of $i_{Lo,k}$, which equals I_o, is more than half the peak current ripple $(\Delta i_{Lo,k})$

$$\Delta i_{Lo,k} = 0.5\left(\frac{V_{Cbus} - nV_o}{nL_o}\right)\left(\frac{D}{2f_s}\right) < I_o \tag{5.24}$$

If Eq. (5.24) is not satisfied, then V_{Cbus} must be recalculated as follows for discontinuous $i_{Lo,k}$:

$$V_{Cbus} = n\left(\frac{V_o + \sqrt{V_o^{\,2} + 16V_o I_o L_o f_s / D}}{2}\right) \tag{5.25}$$

- ***Step 3:*** In order to track the instantaneous input capacitor voltages from t_0-t_2 (decreasing portion), $i_{Lbus,k}$ must be found by applying the value obtained for V_{Cbus} (Eq.(5.23) or Eq.(5.25)) in Step 2 in Eqs. (5.5)-(5.15).

$$i_{Lbus,k}(t) = I_{a,k} - C_a \frac{dv_{Ca,k}}{dt} \tag{5.26}$$

$$i_{Lbus,k}(t) = I_{a,k} + cos\left(B_1(t-t_1)\right)\left(I_{Lbus,k(t1)} - I_{a,k}\right) + \ldots$$

$$\ldots + \left(\sqrt{3}V_{Ca,k(t1)} - V_{Cbus}\right)\left(\sqrt{C_a / L_{bus}}\right)sin\left(B_1(t-t_1)\right) \tag{5.27}$$

where $B_1 = \sqrt{\sqrt{3}/C_a L_{bus}}$, Eqs. (5.26) and (5.27) expresses $i_{Lbus,k}$ from t_0 - t_2. These can then be used to find decreasing portion $v_{Ca,k}$ in the next step.

- ***Step 4:*** Track the instantaneous input capacitor voltages (e.g. $v_{Ca,k}$). The triangle pulse shape of these voltage waveforms needs to be determined; i.e., decreasing and increasing portions must be calculated. The shape is important because it can be used to determine whether $v_{Ca,k}$ is discontinuous at the selected operating point. It is also needed for the following step, which involves using $v_{rec,k}$ to find $v_{Lbus,k}$. The shape of $v_{rec,k}$ is just a reflection of the input capacitor line-to-line voltage waveforms. Simplification of Mode 1 equations together with $i_{Lbus,k}$ obtained in the previous step reveals Eq. (5.28), which gives $v_{Ca,k}$ from t_0 - t_1. Eq. (5.29) gives $v_{Ca,k}$ from t_1 - t_2

$$v_{Ca,k}(t) = \frac{-C_{bus}}{C_a} V_{Cbus} - \frac{C_x}{nC_a} v_{Cx,k}(t) + \left(\frac{I_{a,k}}{C_a} - \frac{I_o}{nC_a}\right)(t - t_0) \tag{5.28}$$

$$v_{Ca,k}(t) = \frac{L_{bus}}{\sqrt{3}} \frac{di_{Lbus,k}}{dt} + V_{Cbus} \tag{29}$$

Eqs. (5.28) and (5.29) can also be used to find the total time needed for input capacitors to discharge. If $t_2 < t_3$ then $v_{Ca,k}$ is discontinuous; else if $t_2 = t_3$, then $v_{Ca,k}$ is at the boundary of continuous and discontinuous voltage, else $v_{Ca,k}$ is continuous. Note that if $v_{Ca,k}$ is discontinuous, then $v_{Ca,k} = 0$ from t_2 - t_3. The increasing portion of $v_{Ca,k}$ can then be calculated using Eq. (5.17).

Once $v_{Ca,k}$ is obtained then to prepare for the next step, the three-phase diode rectifier output voltage $v_{rec,k}$, is found as follows

$$\begin{aligned} v_{Ca,k} > v_{Cb,k} > v_{Cc,k} &\Rightarrow v_{rec,k}(t) = |v_{Ca,k}| + |v_{Cc,k}| \\ v_{Cb,k} > v_{Cc,k} > v_{Ca,k} &\Rightarrow v_{rec,k}(t) = |v_{Cb,k}| + |v_{Ca,k}| \\ v_{Cc,k} > v_{Ca,k} > v_{Cb,k} &\Rightarrow v_{rec,k}(t) = |v_{Cc,k}| + |v_{Cb,k}| \end{aligned} \tag{5.30}$$

where $v_{rec,k}$ depends on the maximum and the minimum phase capacitor voltages.

- ***Step 5:*** With $v_{rec,k}$ known, the voltage across L_{bus} during a full-bridge half-switching cycle k ($v_{Lbus,k}$), can be determined. During Modes 1 and 2 the voltage across L_{bus} is positive and $v_{Lbus,k}$ is

$$v_{Lbus,k}(t) = v_{rec,k}(t - t_0) - V_{Cbus} \tag{5.31}$$

In Mode 3, $v_{rec,k} = 0$ and in Mode 4, current in L_{bus} freewheels through C_{bus} and D_{bus1}; therefore $v_{Lbus,k}$ for Modes 3 and 4 is

$$v_{Lbus,k}(t) = -V_{Cbus} \tag{5.32}$$

After the voltages and currents for the k^{th} full-bridge half-switching cycle are found, the program can be made to sweep through next full-bridge half-switching cycle $k+1$ of the line cycle. The "initial" voltages and currents for $k+1$ will be the "final" voltages and currents found above for k from Steps 1-5. This process can be continued for the line cycle but since $v_{Lbus,k}$ repeats every 60° of the line cycle, only

60° of the line cycle needs to be considered to find the average of v_{Lbus}. There are $n_{sw} = T_l / 3T_s$ ($T_l/6$ = 1/6th of line period and $T_s/2$ = half-switching period) for each 60° section of the line cycle.

- ***Step 6:*** Confirm that the average value of the voltage across inductor L_{bus} ($V_{Lbus(ave)}$) is zero, as it should be if the converter is operating in steady-state. This can be done by checking the integration of $v_{Lbus,k}$ from time t_0 to $T_s/2$ for each k, over n_{sw} number of full-bridge half-switching cycles as follows:

$$V_{Lbus(ave)} = \frac{\sum_{k=1}^{n_{sw}} \int_{t_0}^{T_s/2} v_{Lbus,k}\, dt}{T_l/6} = \frac{\sum_{k=1}^{n_{sw}} \int_{t_0}^{t_2} \left(v_{rec,k} - V_{Cbus}\right) dt - \sum_{k=1}^{n_{sw}} \int_{t_2}^{T_s/2} V_{Cbus}\, dt}{T_l/6} = 0 \qquad (5.33)$$

  If $V_{Lbus(ave)}$ is not zero, then the operating point under consideration is invalid and D, n and/or C_a should be changed to find a valid operating point. Typically converter parameters like n and/or C_a are fixed and it is D that is changed.
- ***Step 7:*** Determine the steady-state input side waveforms such as v_{Ca}, which cannot be determined by considering 1/6th of the line cycle. With the steady-state value of D known, these waveforms can be determined simply by using the above modal equations and sweeping through the full line cycle.
- ***Step 8:*** Repeat the previous steps to determine values for D, n, V_{Cbus}, v_{Ca}, etc. for other sets of component values.

Once such a range has been determined, important converter characteristics can be plotted and a design procedure can be established based on these characteristics.

5.5 Design and Example

Once a range of valid steady-state operating points has been determined, these points can then be plotted as shown in Fig. 5.5, so that the key converter characteristics can be seen. The main characteristics of the converter are the ones related to the DC-bus capacitor voltage V_{Cbus}, instantaneous input capacitor voltage v_{Ca}, the maximum switch voltage $V_{S(pk)}$, transformer primary current i_{Llk} and the maximum switch current $I_{S(pk)}$. These characteristics depend on the selection of duty ratio D, turns ratio n, input capacitor

C_a and the auxiliary capacitor C_x. A procedure for the selection of above components can be developed using the design curves shown in Fig. 5.5.

The procedure will be demonstrated here with an example. For the example, the converter will be designed for the following specifications: line-to-line input rms voltage = 220 $V_{ll(rms)}$, output DC voltage = 48V, maximum output current = 40 A and switching frequency = 25 kHz.

The following should be noted about the design procedure/example and the characteristic curves shown in Fig. 5.5:

- The procedure is based on the computer program described in Section 5.4 of this chapter.
- The procedure is iterative given the interdependency of the key parameters such as D, n and $C_a = C_b = C_c$. Only the final iteration is presented in the design example.
- The operating points in the graphs shown in Fig. 5.5 have been derived for maximum load conditions.
- The operating points in the graphs shown in Fig. 5.5 have been derived, with the assumption that the input line currents are sinusoidal and the input capacitor voltages are discontinuous.
- The design of the DC bus inductor (L_{bus}) and bus capacitor (C_{bus}) is similar to that of most AC-DC converters as they should be designed like a low pass filter to reduce the 360 Hz harmonic component that is present in the single-phase rectifier voltage. The design of these components; therefore is not shown here, but can be calculate using equations given in [19].

5.5.1 Selection of Turns Ratio *n*

The value of n should be such that the converter is able to provide the required V_o. This is not possible if n ($n = n_{pri}/n_{sec}$) is too high. A higher n eventually leads to a higher D as they are proportional to each other according to Eq. (5.23); however, increasing D

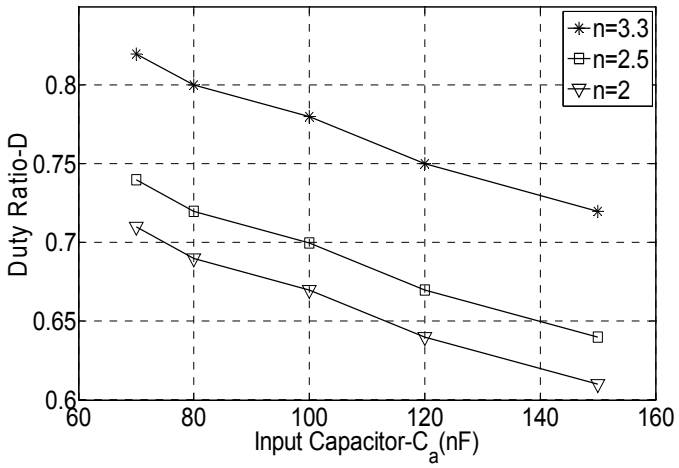
limits the charging time of the input capacitors as the short-circuit time is reduced. An insufficient short-circuit time will lead to the partial charging of the input capacitors and, as a result, the sinusoidal envelope of the input capacitor voltage is affected; therefore the line currents are distorted.

If n is too low, then the transformer primary current will not be extinguished before either S_2 or S_3 is turned off. This is something that cannot be allowed to happen as there is no path for current to flow after S_2 or S_3 is turned off. A smaller value of n will increase the amount of time needed for the primary current to be extinguished, since the smaller n is, the larger the current will be. As a result, the time that can be allowed for this current to extinguish will not be sufficient unless the duration of power transfer mode (and thus the duty ratio D) is reduced.

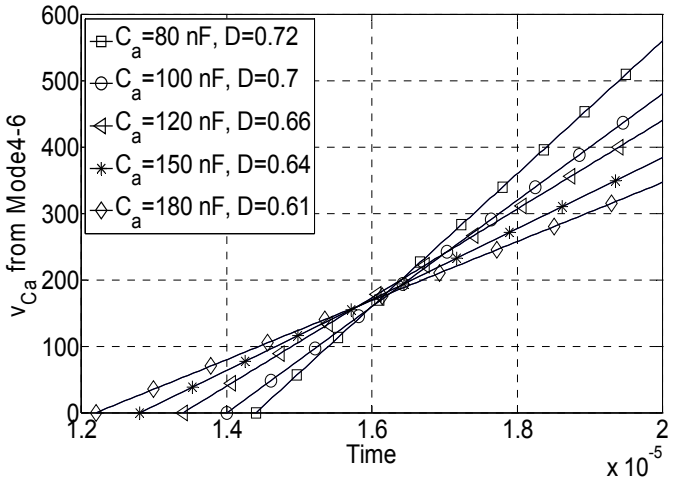
The value of n that is selected; therefore, should not be too large or too small. Fig. 5.5(a) shows a plot of curves to show the relationship among $n - D - C_a$ for three different practically achievable transformer turns ratios, $n = 2$ ($n_{pri}/n_{sec} = 10/5$), $n = 2.5$ ($n_{pri}/n_{sec} = 10/4$) and $n = 3.3$($n_{pri}/n_{sec} = 10/3$), however a designer need not limit the curves to the above n values. For each n the respective curve shows the duty ratio vs. the input capacitor in order to achieve proper voltage regulation at the output and to allow sufficient short-circuit time to extinguish the transformer current before the converter leaves a short-circuit mode. Once n is picked then from Fig. 5.5(a) the respective curve for the selected n can be used to find the operating duty ratio for a selected capacitor in the range 70 nF – 150 nF. A value of $n = 2.5$ is chosen for this iteration.

5.5.2 Determination of Duty Ratio *D* and Input Capacitors C_a, C_b, C_c

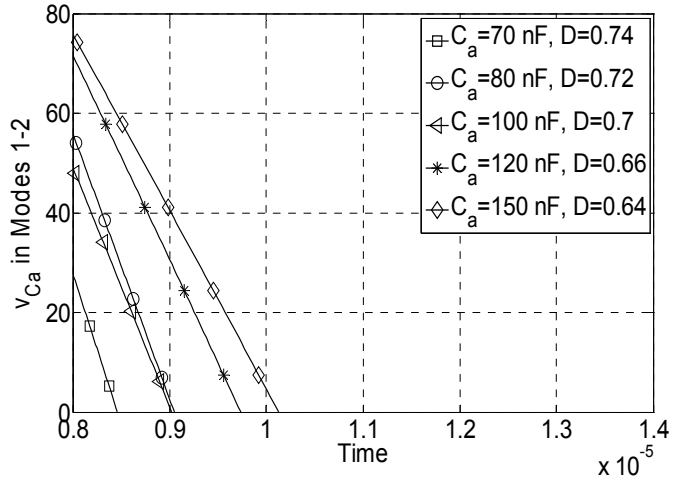
With a value of n selected in the previous step the eligible C_a-D pairs can be read from the curve corresponding $n = 2.5$ in Fig. 5.5(a). Thereafter graphs such as the ones shown in Figs. 5.5(b) and 5.5(c) can be drawn. Fig. 5.5(b) shows a plot of the charging of the input capacitors (Mode 4) when C_a is varied in the range of 70 nF to 150 nF vs. time for suitable D values selected from Fig. 5.5(a). Each curve starts at zero voltage and ramps linearly to its respective peak voltage at $t = 20$ μs; the peak voltage will depend on the charging time allowed and the input capacitor value. The start of charging time ($t = t_3$)



(a). Duty ratio vs. input capacitor for n=3.3, 2.5, 2 [f_s = 25 kHz, P_o =1 .92 kW].



(b) Effect of varying C_a & D on charging time of C_a [n = 2.5, P_o = 1.92 kW].



(c). Effect of varying C_a on discharging time [n = 2.5, P_o = 1.92 kW].

Fig 5.5: Characteristic curves.

for each curve depends on the selected D. According to Fig. 5.5(b), a smaller capacitor will have a higher maximum peak voltage, and thus a higher switch voltage stress. Also a smaller C_a will force a lower short-circuit time as the power transfer mode required will be longer, to ensure proper voltage regulation at the load.

Fig. 5.5(c) shows a graph of curves showing the latter portion of the discharging of the input capacitors, for the same C_a - D combinations found in Fig. 5.5(a) when n = 2.5. If D is too small, then there may not be enough time to discharge the input capacitors, thus resulting in continuous input capacitor voltages and distorted input currents. The continuous voltage mode of C_a can be avoided by making C_a very small, but doing so would result in poor voltage regulation as the energy stored in input capacitors is reduced. On the other hand, if D is too large, then the short-circuit time allowed for the converter is reduced, thus the transformer primary current might not be extinguished

before switch S_2 or S_3 is turned off. Extinguishing the primary current is a must as there is no path for current to flow into the DC bus when the converter moves from a short-circuit mode to an power transfer mode.

Taking these considerations into account, values of D = 0.7 and C_a = 100 nF are selected. According to Fig. 5.5(b), this combination of D, n and C_a will result in $v_{Ca(pk)}$ = 475 V. From Eq. (5.23) V_{Cbus} can be calculated as 171 V, which makes the maximum switch voltage to be

$$v_{S(pk)} = \sqrt{3} v_{Ca(pk)} + V_{Cbus} = 993V \tag{5.34}$$

From Fig. 5.5(c), it can be seen that this combination ensures the input capacitor voltages are discontinuous at full load as it takes around 9.1 μs for C_a to discharge fully in the critical switching cycles (when line current is maximum) which is well within the power transfer mode. Since the input capacitors are selected leaving a considerable margin between the discontinuous voltage mode and the boundary discontinuous voltage mode; v_{Ca} is discontinuous at light loads as well. This is because even though there is less current in the full-bridge to discharge C_a at light load; dv_{Ca}/dt will be high when C_a is low. A good power factor, therefore, can be achieved for a range of loads; however a

"check" to find the harmonics of the line currents using the Fast Fourier Transform (FFT) is needs to done after all the components are selected, as explained at the end of Section 5.5.

5.5.3 Design of the ZVZCS Passive Auxiliary Circuit

With values for n, D and V_{Cbus} known, a value for capacitor C_x, which is the critical component that is needed in order to extinguish the primary current when the converter is operating in short-circuit mode, can be determined. Since the new converter has the same ZVZCS topology as the DC-DC ZVZCS converter proposed in [46], the procedure used in this paper can be used to select C_x and thus will not be repeated here. A value of C_x = 2.5 μF has been chosen as an appropriate value that will extinguish the primary current without unduly increasing the current stress that results from the resonant current hump that is caused by the interaction of C_x and the leakage inductance of the transformer L_{lk}.

5.5.4 Design Determination of Input Inductors L_a, L_b, L_c

The design of the converter in the previous steps is based on the assumption that the input currents are perfectly sinusoidal. In reality, this is not true as these currents will have high–frequency ripple and low–frequency harmonics. As the load is increased, the low–frequency harmonics will be reduced because there is more current available to discharge the input capacitors. This makes it more likely that the input capacitor voltages will be fully discontinuous and thus more likely that the input currents will be sinusoidal.

As a result, it is the high–frequency ripple that is more dominant when the converter is operating with heavy load.

Fig. 5.6 shows a per phase equivalent circuit of L–C filter section that can be used to find the relationship between C_a, L_a and the line current harmonics. L_a and C_a refer to the input filter components of phase A, that are used to filter out undesired harmonics. If f_r is the dominant harmonic frequency (sidebands) related to the switching frequency f_s and line frequency f_l, then f_r can be written as $f_r = 2fs \pm f_l$. Eq. (35) gives the allowed high frequency input ripple current in to the utility side (I_{lfr}) as a function of total generated harmonics (I_{tfr}) and input parameters

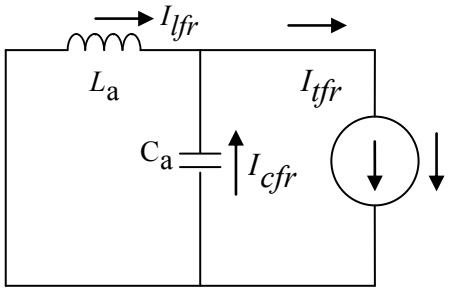


Fig 5.6: Single-phase equivalent L-C filter circuit.

$$I_{lfr} = I_{tfr}\left(\frac{\frac{1}{2\pi f_r C_a}}{2\pi f_r L_a - \frac{1}{2\pi f_r C_a}}\right) \tag{5.35}$$

If $I_{lfr} = 20\%I_{tfr}$, then the relationship between the input filter components and harmonic content becomes

$$L_a C_a = \left(\frac{1}{2\pi f_r}\right)^2 \left(1 + \frac{I_{tfr}}{0.2 I_{tfr}}\right) \tag{5.36}$$

where C_a = 100 nF and f_r = 49940 Hz or 50060 Hz. L_a becomes 600 μH.

The final step of the procedure is to confirm that the converter's input line currents comply with required harmonic standards, such as IEC 61000–3–2 Class A, for the worst–case conditions.

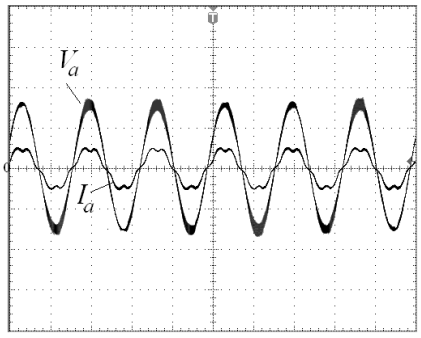
The converter's input line currents are most likely to be distorted when operating under light load conditions as there is less current available to discharge the input capacitors' voltages, so that these voltages are not fully discontinuous. The converter's operation should be confirmed against the IEC standard for a variety of load conditions. This can be done using the computer program that was developed in Section III. The worst-case load for meeting the Class A standard was found to be 0.4 kW; if the standard can be met with this load, it can be met at lighter loads. Since IEC 61000–3–2 Class A is an absolute standard and is not relative to the load, it can be met when the converter is

operating under much lighter load conditions, even though the input currents may be significantly distorted because the current levels are very small.

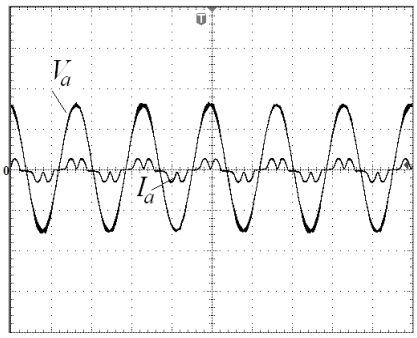
5.6 Experimental Results

An experimental prototype of the fundamental buck-based full-bridge converter under study was built to confirm its feasibility. It was built for an input line-line voltage of 220 V, an output voltage of 48 V, a maximum output current of 40 A and a switching frequency of 25 kHz. The converter was designed with FGA25N120FTD as switches, DSEI60-12A-ND as three-phase rectifier diodes and FFA40UP35STU-ND devices as output side diodes. The converter was implemented with $L_a = L_b = L_c = 600$ µH, $C_a = C_b = C_c = 100$ nF, $L_{bus} = 760$ µH, $C_{bus} = 1500$ µF, $C_x = 2.5$ µF, $L_o = 460$ µH, $C_o = 1500$ µF and $n = 2.5$.

Figs. 5.7(a) and (b) show input phase current and voltage waveforms when the converter is working at 1.92 kW and at 0.4 kW. Table I shows the harmonics of the input line current (I_a) under different load conditions as well as the input power factor. The input line currents meet the IEC standard for the entire load range and the converter has near unity power factor at higher loads.



(a) $P_o = 1.92$ kW, pf = 0.99 ($V_a = 100$ V/div, $I_a = 20$ A/div, $t = 10$ms/div).

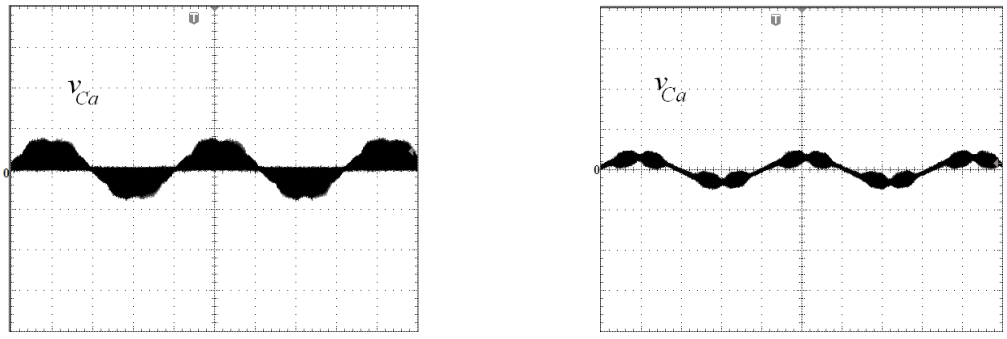


(b) $P_o = 400$ W, pf = 0.89 ($V_a = 100$ V/div, $I_a = 10$ A/div, $t = 10$ms/div).

Fig 5.7: Experimental Input voltage and current.

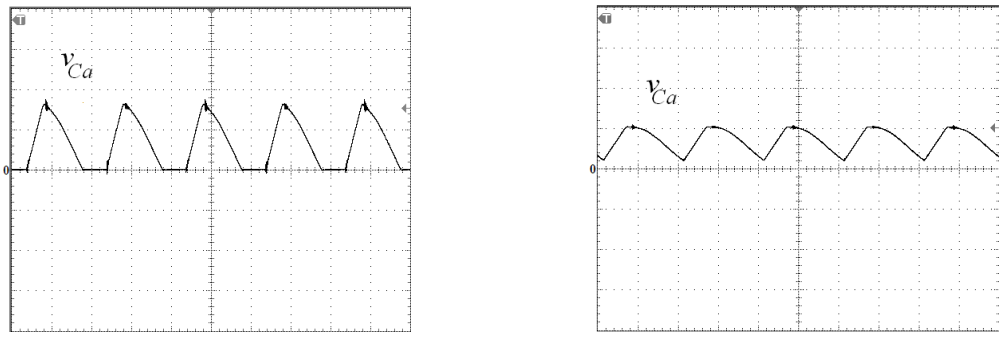
Figs. 5.8 and 5.9 show experimental waveforms of the voltage across an input capacitor for different loads, for several line cycles (Fig. 5.8) and several switching cycles (Fig. 5.9). It can be seen that this voltage (v_{Ca}) is discontinuous throughout the line cycle for heavy load, but is continuous for significant parts of the line cycle for light load. The more discontinuous the voltage is the less distortion appears in the input current**.** It should be noted that the boundary load, the load at which an input capacitor voltage such as v_{Ca} goes from being fully discontinuous to being continuous for some of its switching cycles and vice versa is approximately 1.2 kW.

Fig. 5.10 shows various experimental waveforms of the DC side of the converter. Fig. 5.10(a) shows the output voltage (v_{rec}) and the output current (i_{rec}) of the three-phase diode rectifier. It can be seen that the voltage is triangular, which is caused by the charging and discharging of the input capacitors, and the current consists of square



(a) (b)

Fig 5.8: Input capacitor phase voltage P_o = (a) 1.92 kW and (b) 0.4 kW (v_{Ca} = 500 V/div, t = 4 ms/div).

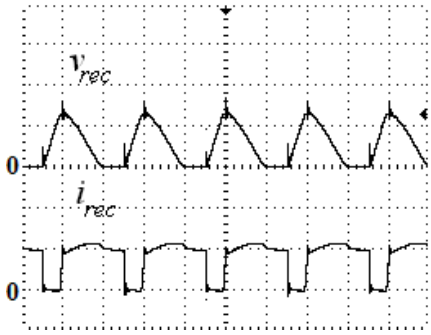


(a) (b)

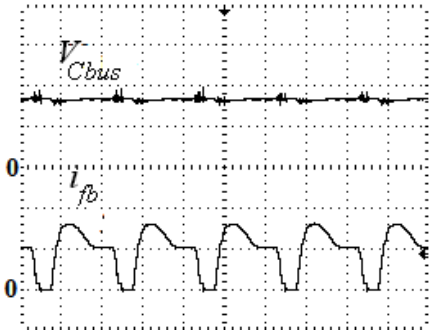
Fig 5.9: Input capacitor phase voltage P_o= (a) 1.92 kW and (b) 0.4 kW (v_{Ca} = 250 V/div, t = 10 μs/div).

pulses, with the peak current determined by the current through L_{bus}.

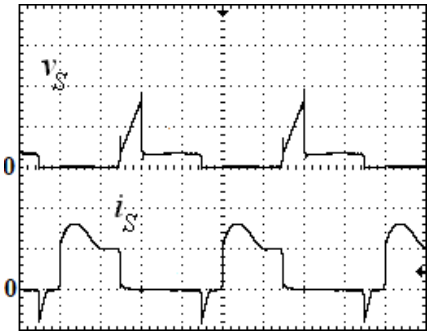
Fig. 5.10(b) shows the voltage across C_{bus} (V_{Cbus}) and the current that enters the full-bridge (i_{fb}). It can be seen that the DC bus voltage is stepped down from the input and is approximately 170 V and that the current has a hump that is caused by the resonant interaction between the L_{lk} and C_x when the converter enters an energy-transfer mode. Fig. 5.10(c) shows a typical switch voltage (v_S) and switch current (i_S). It can be seen that the switch voltage has a triangular part, which corresponds to when the input capacitors



(a). Output voltage & current of the three-phase rectifier (v_{rec} = 500 V/div, i_{rec} = 10 A/div, t = 10 µs/div).



(b). C_{bus} voltage & current entering the full-bridge (V_{Cbus} = 100 V/div, i_{fb} = 20 A/div, t = 10 µs/div).



(c). Voltage & current of a converter switch (v_S = 500 V/div, i_S = 20 A/div, t = 10 µs/div).

Fig 5.10: Experimental waveforms.

are charging, and a flat part, which corresponds to when C_{bus} is placed in the DC bus. According to Fig. 5.10(c) maximum switch voltage around 950 V and the maximum switch current is around 35 A. The maximum efficiency of the prototype was 80%, as shown in Table 5.1.

The prototype efficiency can be explained by the fact that converter operation was simplified for a better study of the properties and characteristics of the new converter, but that this was done at the expense of performance. The experimental prototype that was built was a simple, proof–of–concept model that was used to investigate and confirm the theories discussed in this paper - to show that it is possible to implement a buck–based, three–phase AC–DC, single–stage full–bridge converter that can achieve three–phase AC–DC power factor correction with continuous input and output currents using just standard phase–shift PWM.

With respect to efficiency, the buck converter examined in this chapter shares the same properties as other converters that do not have a bulk capacitor across their DC bus at all times, such as the basic single-stage boost converter shown in Fig. 5.11, which also does not have a C_{bus} to clamp spikes whenever its switches turn off. As a result, the fundamental single-stage boost converter shown in Fig. 5.1 is rarely implemented without some sort of active snubber or soft-switching method. There is, therefore, little discussion in the literature about the efficiency of this converter when implemented with dissipative RC snubbers. On the rare occasions when this has been done, such as in [52]-[54] for a single-phase input, the maximum efficiency was reported to be around 70-80%, which is

Table 5.1: IEC 61000-3-2 CLASS A, INPUT CURRENT HARMONICS, POWER FACTOR AND EFFICIENCIES

Harmonics	Class A	1.96 kW	1.44 kW	0.96 kW	400 W
5^{th}	2.06	0.53	0.33	0.41	0.38
7^{th}	1.39	0.04	0.01	0.16	0.18
11^{th}	0.60	0.05	0.03	0.05	0.04
13^{th}	0.38	0.02	0.01	0.04	0.05
Power Factor		0.99	0.99	0.97	0.89
Efficiency		70%	72%	77.7%	80%

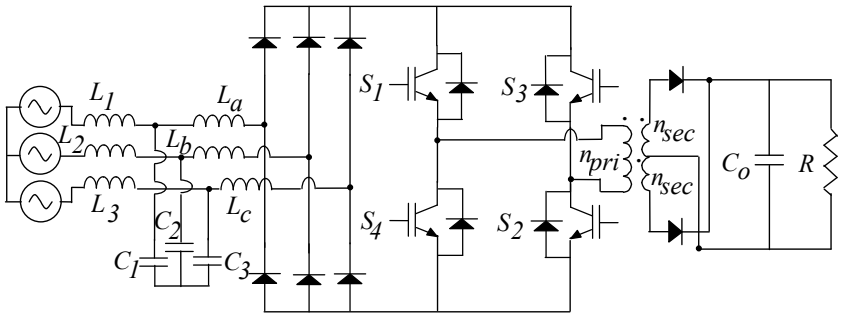


Fig 5.11: Three-phase AC-DC single-stage isolated boost converter.

in line with what was found with the experimental prototype.

An example of the difference that the use of soft-switching can make in a current-fed full-bridge boost converter when compared to using RC snubbing can be found in [54]. Although the boost converter in that paper was used for a low input DC voltage high output voltage application, nonetheless an efficiency improvement of about 10% was reported. It is expected that a similar significant efficiency improvement can occur if soft-switching is implemented in the new converter.

Such efficiency improvement was actually been reported in [44], for a three- phase, two-switch forward buck-type converter, which can be considered to have similar basic operation to the buck-type full-bridge converter that is the focus of this paper. In this converter, an energy recovery circuit was connected to the DC bus and resonant elements were added to the base converter to transform it into a ZCS variable frequency converter. A maximum converter efficiency of 90% was reported in [44].

5.7 Conclusion

In this chapter, a new three-phase AC-DC, single-stage high power factor PWM full-bridge converter was presented, Its steady-state operation was explained and analyzed and experimental results obtained from a prototype converter that was designed according to a design procedure confirmed its feasibility. Unlike most previously proposed three-phase single-stage converters the proposed converter has a buck converter (capacitive input filter) input section. As a result, the converter does not suffer from high

input ripple as its input currents are continuous without high current peaks, and current is continuous due to output filter inductor. Also, the converter can achieves a good power factor without using additional controllers or current sensors; thus the cost is low.

The main objective of this chapter was to examine a buck-based three-phase single-stage converter in its simplest form – with fixed frequency PWM operation and with no soft-switching circuitry – to gain insight into the nature of buck-based single-stage converters. As a result, the efficiency of the converter was low compared to what is typically accepted; efficiency improvement through the use of soft-switching methods can be the subject of future work.

Chapter 6

6 Comparison of Two Buck–Type Three–Phase Single–Stage AC–DC Full Bridge Converters

6.1 Introduction

In Chapter 5, a new three-phase AC-DC single-stage converter that was based on a buck converter front-end section was examined. This chapter continues the work of the previous chapter by investigating the properties and characteristics of a modification version of that converter (henceforth referred to as Converter #2) and comparing them to those of the original converter (henceforth referred to as Converter #1) discussed in Chapter 5. As in Chapter 5, the operation of the modified converter, Converter #2, is explained in detail, its steady-state characteristics are determined by mathematical analysis, the results of the analysis are used to develop a design procedure for the selection of key components, and the procedure is demonstrated with an example that was used to design a prototype converter from which experimental results were obtained. The chapter concludes with a direct comparison of the two converters in terms of such properties as switch stress, input power factor and efficiency.

6.2 Steady-State Operation of Converter #2

Converter #1, which was the subject of Chapter 5, and Converter #2, which is a modified version of that converter, are shown in Fig. 6.1 and 6.2, respectively. The following should be noted:

- Converter #2 has almost the same topology as Converter #1 and operates according to the same basic fundamental principles that were described in Chapter 5. The only difference is the presence of a bulk capacitor (C_{bus}) across the DC bus during certain modes of operation of Converter #1 as Converter #2 lacks this capacitor. The absence of C_{bus} from Converter #2 means that the bus voltage is not a DC waveform, but is the directly output of the input diode bridge. C_{bus} in Converter #1 however, is not connected across the DC bus when the full–bridge converter is in a

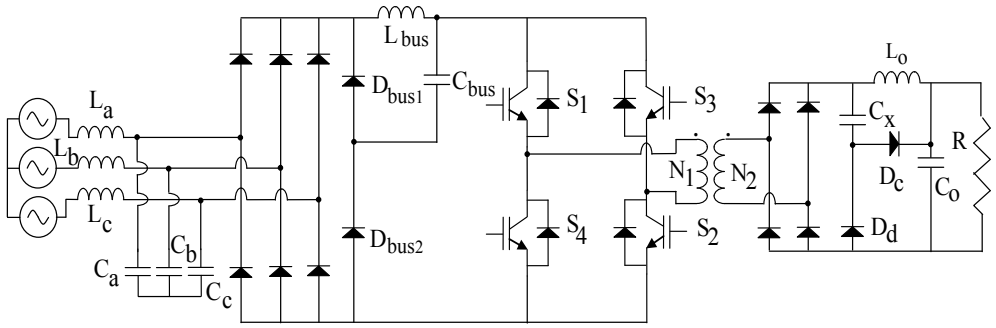


Fig 6.1: Three–phase AC–DC, single–stage buck–type full–bridge converter.

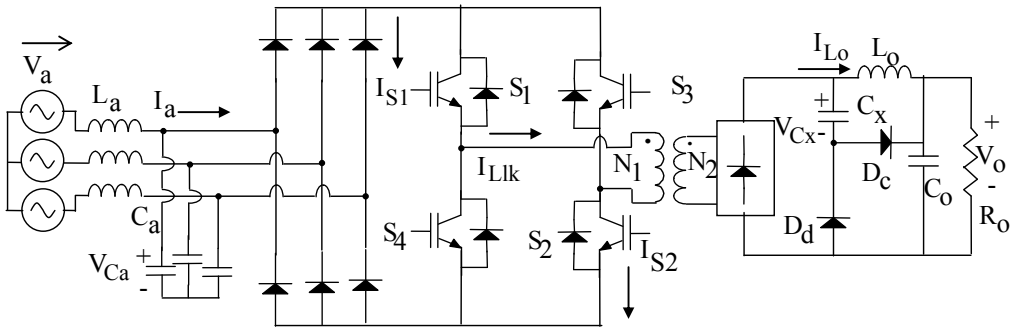


Fig 6.2: Three–phase AC–DC, single–stage modified buck–type full–bridge converter [55].

freewheeling mode of operation and thus the charging of the input capacitors of the two converters are the same.

- The comparison that is considered in this chapter is a comparison between the two three–phase single–stage full–bridge converters shown in Figs. 6.1 and 6.2, both of which do not have a bulk capacitor across their DC bus at all times that can clamp spikes whenever their switches turn off. As a result, both converters should be implemented with some sort of active snubber or soft–switching method in practice, as in the two–switch forward converter [44], which combines an energy–recovery circuit with resonant converter soft–switching techniques. Since the main focus of this chapter is to compare the properties of the two converters, the use of resonant and other soft–switching techniques would obscure the basic fundamental

properties of the converters and thus both converters are considered as hard–switching converters in this chapter, as was done in Chapter 5.

Fig. 6.3 shows equivalent circuit diagrams that illustrate the modes of operation that the Converter #2 goes through during a half switching cycle, and Fig. 6.4 shows typical converter waveforms. In Fig. 6.4, the output capacitor and load are shown as an equivalent voltage source and the k^{th} switching cycle where $v_{a,k} = V_{ph(pk)}$, $v_{b,k} = v_{c,k} = -V_{ph(pk)}/2$ is considered. The assumptions made here are similar to those made in the previous chapter and are thus not repeated here.

Mode 1 ($t_0 < t < t_1$), [Fig. 6.3(a)]:

Before $t = t_0$, S_1 and S_3 are on, the input capacitors are charged to their peak voltages as determined by the line currents for k, the auxiliary circuit capacitor C_x is at its minimum voltage $V_{Cx,k(min)}$, and there is no current flowing in the full–bridge. At $t = t_0$, S_3 is turned off and S_2 is turned on and the three–phase diode rectifier output current $i_{bus,k}$, starts flowing into the full–bridge. $i_{bus,k}$ is the sum of the line current $I_{a,k}$ and the discharging current of the input capacitor C_a ($i_{Ca,k}$). $i_{bus,k}$ goes through the switches and the transformer primary and equals the leakage inductor, L_{lk} current $i_{Llk,k}$. The transformer secondary current charges C_x through diode D_c during this mode. Mode 1 ends when input capacitors are fully discharged.

The input capacitors discharge during Mode 1 from its initial value $V_{Ca,k(t0)}$ until $v_{Ca,k}$ reaches zero at $t = t_1$. The difference between the $i_{Llk,k}$ and $I_{a,k}$, gives the increasing current injected by input capacitor C_a. The discharging of C_a can be expressed as

$$i_{Llk,k} - I_{a,k} = -C_a \frac{dv_{Ca,k}}{dt} \tag{6.1}$$

The output voltage of the three–phase diode bridge at $t = t_0$ is the line–line input capacitor voltage; therefore, $v_{rec,k} = \sqrt{3} v_{Ca,k}$. The relation between $v_{Ca,k}$, $v_{Cx,k}$ and $i_{Llk,k}$ can be expressed as

$$\sqrt{3}v_{Ca,k} - n(v_{Cx,k} + V_o) = L_{lk}\frac{di_{Llk,k}}{dt} \tag{6.2}$$

where V_o is the DC output voltage and n is the ratio between primary turns to secondary turns of the transformer. At the transformer secondary side, C_x is charged by a current that equals the difference between the secondary current and the load current $I_{o,}$ according to

$$ni_{Llk,k} - I_o = C_x\frac{dv_{Cx,k}}{dt} \tag{6.3}$$

Eqs. (1) – (3) are combined to give the following equation for $v_{Ca,k}$

$$C_aC_xL_{lk}\frac{d^3v_{Ca,k}}{dt^3} + (n^2C_a + \sqrt{3}C_x)\frac{dv_{Ca,k}}{dt}) - n^2I_{a,k} + nI_o = 0 \tag{6.4}$$

where the initial conditions are

$$V_{Ca,k(t0)} = \frac{I_{a,k}(1-D)T_s}{2C_a} \qquad \text{(6.5a)}, \quad \left(\frac{dv_{Ca,k}}{dt}\right)_{t=t0} = 0 \tag{6.5b}$$

The solution to Eq. (6.4) yields

$$v_{Ca,k} = V_{Ca,k(t0)} + \frac{a_3}{a_2}(t-t_0) - \frac{a_3}{a_2}\sqrt{\frac{a_1}{a_2}}\sin\left(\sqrt{\frac{a_2}{a_1}}(t-t_0)\right) \tag{6.6}$$

Substituting Eq. (6.6) into Eq. (6.1) gives

$$i_{Llk,k} = I_{a,k} + \frac{a_3}{a_2}C_a - \frac{a_3}{a_2}C_a\cos\left(\sqrt{\frac{a_2}{a_1}}(t-t_0)\right) \tag{6.7}$$

where $a_1 = C_aC_xL_{lk}, a_2 = \sqrt{3}C_x - n^2C_a, a_3 = nI_o - n^2I_{a,k}$. Substituting Eq. (6.7) into Eq. (6.3) gives

$$v_{Cx,k} = V_{Cx(t0)} + \frac{n}{C_x}\left(I_{a,k} + \frac{a_3}{a_2}C_a - \frac{I_o}{n}\right)(t - t_0) - \frac{nC_a}{C_x}\frac{a_3}{a_2}\sqrt{\frac{a_1}{a_2}}\sin\left(\sqrt{\frac{a_2}{a_1}}(t - t_0)\right) \quad (6.8)$$

Mode 2 ($t_1 < t < t_2$), [Fig. 6.3(b)]:

At $t = t_1$, the input capacitors are fully discharged and $v_{rec,k}$ is zero while capacitor C_x continues to be charged. As the input capacitors stop discharging at $t = t_1$, $i_{bus,k}$, takes a step change from its peak to $I_{a,k}$ as shown in Eq. (9),

$$i_{bus,k} = \begin{cases} I_{a,k} + i_{Ca,k}, t \le t_1 \\ I_{a,k}, t > t_1 \end{cases} \quad (6.9)$$

Although $i_{bus,k}$ can take a step change, $i_{Llk,k}$ cannot change suddenly due to L_{lk}. The step change in $i_{bus,k}$ is the difference between the currents $i_{bus,k}$ and $i_{Llk,k}$ and is conducted by the body diodes of the switches S_3 and S_4 which are currently off. The body diodes are not reversed biased because the bus voltage is zero during Mode 2. During this mode, $i_{Llk,k}$ decreases due to a counter voltage impressed across L_{lk} by C_x.

At some time during this mode, the leakage inductor current becomes the same as the reflected secondary current. C_x reaches its peak voltage and diode D_c stops conducting. Diode D_d starts to conduct and C_x begins to discharge to bridge the gap between I_o and the secondary current. At the end of this mode, the primary current drops to a level that matches $i_{bus,k}$. S_1 is turned off at $t = t_3$ and the body diode of S_4 begins to conduct.

By applying $t = t_1$ in Eq. (6.7), the initial condition for $i_{Llk,k}$ for Mode 2 can be obtained. The presence of the counter voltage across L_{lk} diminishes $i_{Llk,k}$ during Mode 2 according to

$$nv_{Cx,k} = L_{lk}\frac{di_{Llk,k}}{dt} \quad (6.10)$$

Combining Eqs. (6.3) and (6.10) gives the following result:

$$nC_x L_{lk} \frac{d^2 i_{Llk,k}}{dt^2} + n i_{Llk,k} - I_o = 0 \tag{6.11}$$

The solution to this equation is

$$i_{Llk,k} = -I_{Llk,k(t1)} \cosh\left(\sqrt{\frac{n}{a_4}}(t - t_1)\right) + \left(\frac{I_o}{n}\sqrt{\frac{a_4}{n}}\right)\sinh\left(\sqrt{\frac{n}{a_4}}(t - t_1)\right) - \frac{I_o}{n} \tag{6.12}$$

where $a_4 = C_x L_{lk} / n$. Eqs. (6.10) and (6.12) are used to determine $v_{Cx,k}$ for this mode as follows:

$$v_{Cx,k} = L_{lk}\left(\frac{I_{Llk,k(t1)}}{\sqrt{na_4}}\sinh\sqrt{\frac{n}{a_4}}(t - t_1) - \frac{I_o}{n^2}\cosh\sqrt{\frac{n}{a_4}}(t - t_1)\right) \tag{6.13}$$

Mode 3 ($t_2 < t < t_3$), [Fig. 6.3(c)]:

At $t = t_2$, C_x begins to discharge to bridge the gap between the load current I_o and the secondary current. At the end of this mode, the primary current drops to a level that matches the DC bus current, $i_{bus,k}$ and the body diodes of switches S_3 and S_4 will stop conducting thereafter. Towards the end of this mode, S_1 is turned off, the switch capacitors across S_1 and S_4 begin to charge and discharge respectively using $i_{Llk,k}$. At $t = t_3$ the switch capacitor of S_4 is completely discharged and the body diode of S_4 starts to conduct.

Capacitor C_x discharges according to

$$-\left(I_o - n i_{Llk,k}\right) = C_x \frac{dv_{Cx,k}}{dt} \tag{6.14}$$

and $i_{Llk,k}$ continues to decrease according to Eq. (10).The modal equations for Mode 3 are thus the same as those for Mode 2.

Mode 4 ($t_3 < t < t_4$), [Fig. 6.3(d)]:

At $t = t_3$, the line currents start to flow into the input capacitors and they begin to

charge as follows:

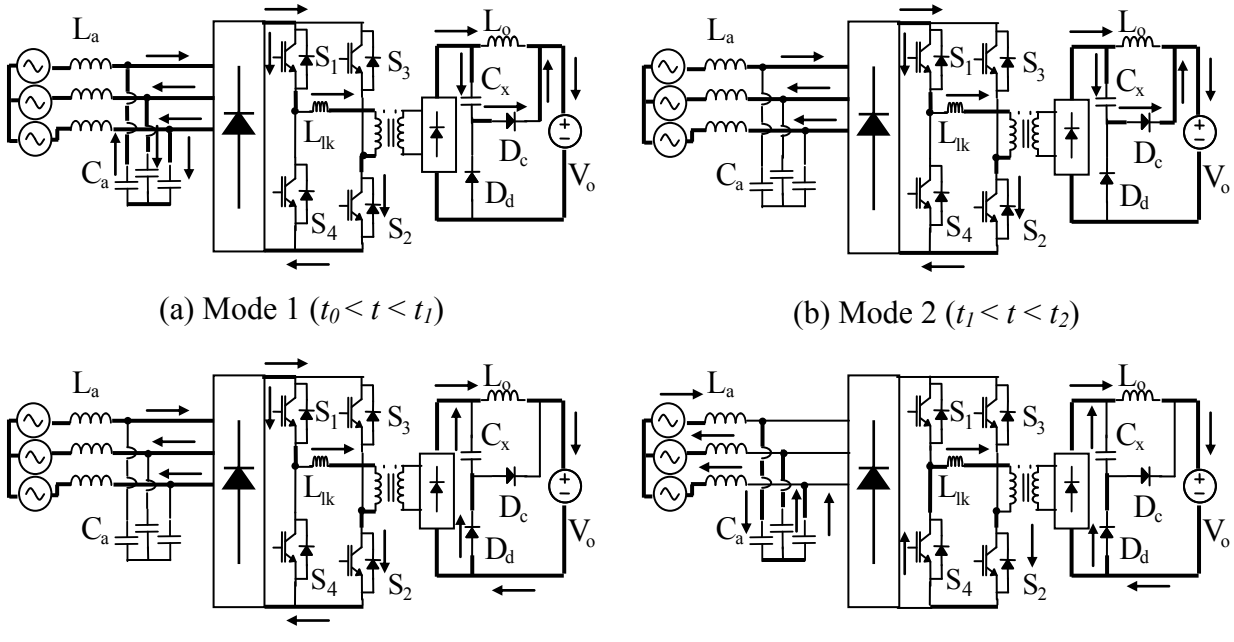
$$I_{a,k} = C_a \frac{dv_{Ca,k}}{dt} \tag{6.15}$$

The solution to Eq. (15) is

$$V_{Ca,k} = \frac{I_{a,k}}{C_a}\left(t - t_3\right) \tag{6.16}$$

$i_{Llk,k}$ freewheels through the two bottom switches and continues to decrease due to the counter voltage impressed by C_x, and falls to zero (Eqs. (6.12) and (6.13)) and there is no current freewheeling in the full–bridge thereafter. After $i_{Llk,k}$ is fully extinguished C_x discharges linearly, providing the entire load current since the secondary current is zero, according to

$$-I_o = C_x \frac{dv_{Cx,k}}{dt} \tag{6.17}$$



(a) Mode 1 ($t_0 < t < t_1$)

(b) Mode 2 ($t_1 < t < t_2$)

(c) Mode 3 ($t_2 < t < t_3$)

(d) Mode 4 ($t_3 < t < t_4$)

Fig 6.3: Modes of operation of Converter #2 at steady–state.

The solution to Eq. (6.17) is

$$v_{Cx,k} = v_{Cx,k(t5)} - \frac{I_o}{C_x}(t - t_3) \tag{6.18}$$

At $t = t_4$, C_a reaches its peak voltage for k, C_x reaches its minimum voltage for k, and the next half switching cycle $k+1$ begins.

6.3 Analysis of Converter #2

An analysis of the steady–state characteristics of Converter #2 is needed to determine it operates for any given set of specifications (line–to–line input voltage: $V_{ll(rms)}$, output voltage: V_o, output current: I_o, and switching frequency: f_s) and for a selected set of parameters (input capacitors: C_a, duty ratio of the full–bridge: D, transformer turns ratio: $n = n_{pri}/n_{sec}$, leakage inductance: L_{lk}, auxiliary capacitor: C_x and the output inductor: L_o). Important converter characteristic graphs can be plotted as a result of the analysis and then used to develop a design procedure, which will be done in the next section of this chapter.

The analysis of Converter #2 presented in this chapter is very similar to the analysis presented in Chapter 5 for Converter #1. In both cases, steady–state operating points for various combinations of parameter values and component values can be determined by checking the net average voltage across an inductor of each converter. For example, in the case of the converter shown in Fig. 6.1, the status of the converter is checked by evaluating the average value of the L_{bus} voltage, over a period of $1/6^{th}$ of a 60 Hz line cycle (an interval of 60º of the fundamental period is used due to symmetries). If the average voltage of L_{bus} is zero for this period, then the converter is in steady–state and a steady–state operating point has been determined. In order to calculate the average value, the instantaneous L_{bus} voltage ($v_{Lbus,k}$) waveform during any k full–bridge half switching cycle can be found by the difference between the three–phase diode bridge rectifier output voltage and the voltage across capacitor C_{bus} ($v_{Lbus,k} = v_{rec,k} - V_{Cbus}$). The modal equations help to find the variables $v_{rec,k}$ and V_{Cbus}. If the average voltage across L_{bus} is not zero, then steady–state operating points can be determined by varying the converter

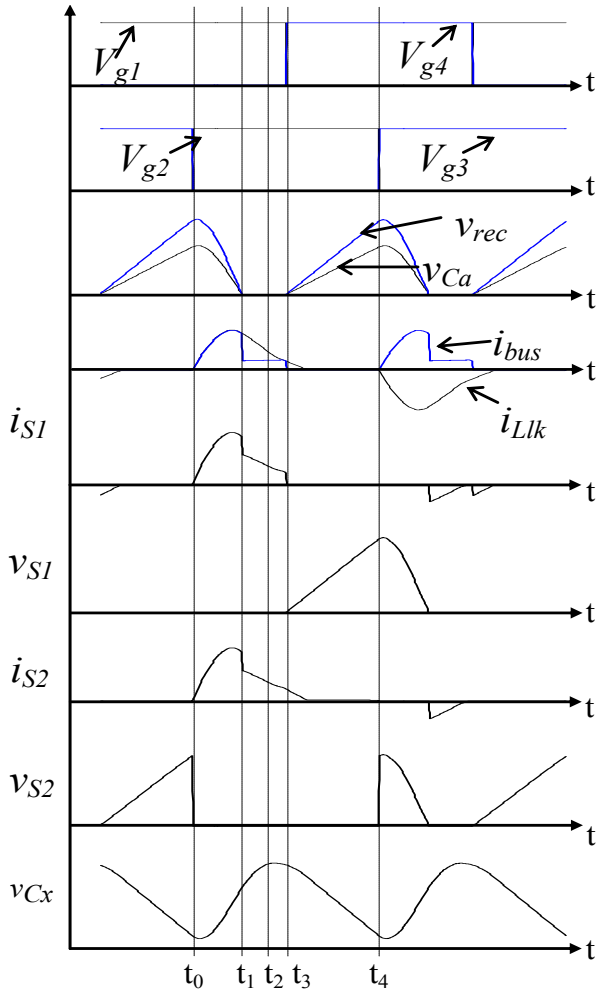


Fig 6.4: Typical waveforms for Converter #2.

parameters (duty–cycle, input capacitor, transformer turns ratio etc.) until the steady–state criteria is met.

In the case of the converter in Fig. 6.2, which does not have a DC bus inductor, a similar matching method can be used except that it is done with the transformer leakage inductor (L_{lk}) – the average value of the voltage across this inductor must be zero after $1/6^{th}$ of the 60 Hz input line cycle. Since the analyses of the two converters are very similar, the analysis of Converter #2 (Fig. 6.2) is not presented in this chapter and interested readers are referred to the analysis presented in Chapter 5 for Converter #1 (Fig. 6.1) instead.

6.4 Design Procedure of Converter #2

Once a range of valid steady–state operating points for the converter shown in Fig. 6.2 has been determined by analysis, these points can then be plotted as shown in Fig. 6.5, which shows several plots that indicate the variation of converter key characteristics when parameters are changed. The main characteristics of the converter are the instantaneous input capacitor voltage v_{Ca}, peak switch voltage stress $V_{s(pk)}$ and instantaneous transformer primary current $i_{Llk,k}$. These characteristics depend on the selection of the duty ratio D, turns ratio n, input capacitor C_a, leakage inductor L_{lk} and auxiliary capacitor C_x. A procedure for the selection of these parameters can be developed using the design curves shown in Fig. 6.5.

The procedure is demonstrated below with an example. The converter is designed for the following specifications: Line–to–line input voltage = 220 V, output voltage = 48 V, maximum output current = 40 A, switching frequency = 25 kHz. The procedure is iterative given the interdependency of the key parameters. Only the final iteration is presented in the design example.

6.4.1 Selection of Turns Ratio *n*

Two factors must be considered when picking a value for n. The first factor is the ability of the converter to regulate the output DC voltage as specified (V_o = 48 V). This is not possible if $n = n_{pri}/n_{sec}$ is too high. The second factor is the reflected load current to the transformer primary side, which should be low. If n is too small, then i_{Llk} may not be sufficiently extinguished before S_2 or S_3 is turned off (when the converter exits a freewheeling mode) and a longer freewheeling time is needed to apply the counter voltage across L_{lk}. This is not desirable since if too much freewheeling time is needed, D of the converter must be decreased and the converter will not be able to produce the desired V_o.

The value of n that is selected should be the smallest value that allows the converter to deliver the required V_o and that allows for the selection of the other parameters. For this iteration, a value of n = 2.5 is selected based the fact that this value offers the most possible valid combinations of component values, as seen by characteristic curves like

the ones in Fig. 6.5. It should be noted that characteristic curves with values of n that are different than 2.5 can be generated in a similar manner, but only those for n = 2.5 are shown in Fig. 6.5.

6.4.2 Determination of Duty Ratio D and Input Capacitors $C_a = C_b = C_c$

If D is too small, then the power transfer mode is shortened and the converter's operation is affected in two ways. First, the converter may not be able to provide the required V_o. Second, there may be insufficient time for the input capacitors to fully discharge, which would result in their voltages not being fully discontinuous so that low frequency harmonics will appear in the input currents. This problem may be avoided if $C_a = C_b = C_c$ is chosen to be very small, which would ensure that the input capacitors do fully discharge. Doing so, however, would also result in excessively high values of $V_{Ca(pk)}$ and therefore peak switch voltage $V_{s(pk)}$, as $V_{s(pk)} = \sqrt{3}V_{Ca(pk)}$.

If D is too large, then the time allocated for the input capacitors to charge up will be inadequate and therefore partial charging will result. As a result, the input capacitors will not store sufficient energy to transfer to load during the power transfer modes, which ultimately affect the converter's voltage regulation.

A value of n = 2.5 was selected in the previous step. As D should not be too small or too large, a value of D = 0.5 is considered. Fig. 6.5(a) is a graph of curves of voltage $v_{Ca,k}$ vs. time for different values of C_a (50 nF $\leq C_a \leq$ 300 nF) and with D = 0.5, n = 2.5, L_{lk} = 35 μH (as determined from the previous iteration) and $I_{a(pk)}$ = 7.5 A, which is the maximum peak current. At time t = 0, all $v_{Ca,k}$ curves are shown to be zero, and all rise as time is increased; this shows the charging of C_a during the freewheeling mode.

Figs. 6.5(b) and (c) contain graphs of curves that are similar to those in Fig. 6.5(a) except that they show the discharging of C_a (i.e. the curves begin with values of $V_{Ca(pk)}$ at time t = 0, then approach zero as the time is increased). These graphs indicate the time taken by C_a to discharge during Mode 1 for C_a (50 nF $\leq C_a \leq$ 300 nF) at full–load (P_o = 1.92 kW) and at half–load respectively. Full–load operation is considered to minimize input current harmonic content when the converter is operating with maximum input

current. Half–load operation is considered because if $v_{Ca,k}$ is discontinuous at half–load, then it is likely that the converter will meet the IEC 61000–3–2 Class A standard for lighter loads.

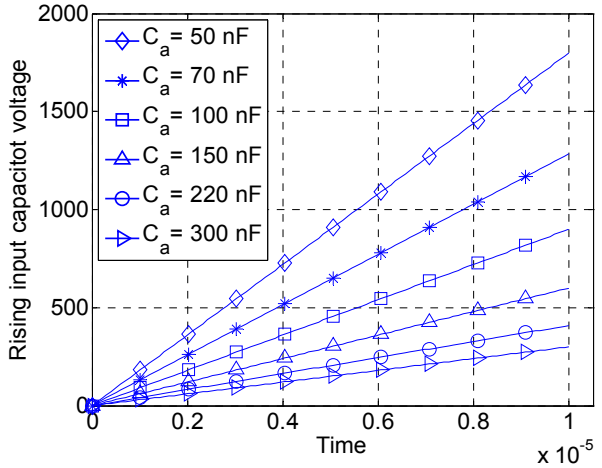
Curves like the ones shown in Figs. 6.5(b) and (c) can be drawn for a range of values of D starting from D = 0.5(i.e. D = 0.55, 0.6...) if necessary. According to Fig. 6.5(b), $v_{Ca,k}$ curves are discontinuous for C_a (50 nF ≤ C_a ≤ 300 nF) under full–load conditions as all the curves reach 0 V well before $DT_s/2$ = 10 μs. Since $V_{s(pk)}$ is related to $V_{Ca(pk)}$, and since it can be seen from Fig. 6.5(a) that this voltage is reduced as C_a is increased; therefore, the larger the value of C_a, the lower the capacitor voltage and switch stress will be. However, it can be seen from Fig. 6.5(c) that if C_a = 300 nF and if P_o = 0.96 kW then $v_{Ca,k}$ will not be able to drop to zero before $DT_s/2$ = 5 μs (where half load duty is assumed to be D/2) and thus $v_{Ca,k}$ will be continuous, but $v_{Ca,k}$ can drop to zero within this time if C_a = 220 nF. C_a = 220 nF can therefore be considered as a possible selection, in conjunction with D = 0.5 for this iteration.

Whether the required correct V_o can be achieved by this operating point must be confirmed; if V_o < 48, then D must be increased and C_a should be selected accordingly. It can be seen from Fig. 6.5(a) that the selected C_a charges to a peak voltage of 400 V; since $V_{s(pk)} = \sqrt{3} V_{Ca(pk)}$, therefore $V_{s(pk)}$ = 693 V.

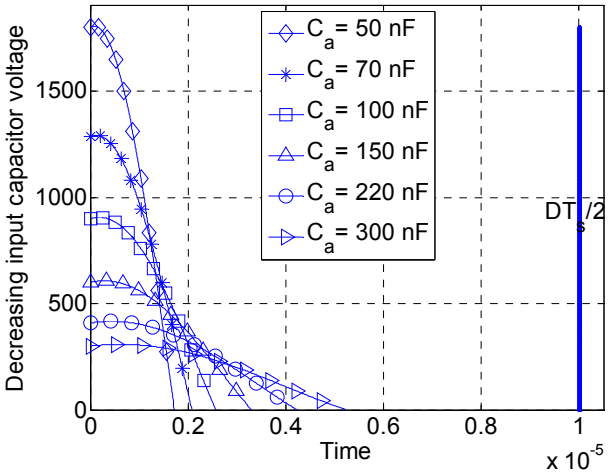
With the values of n = 2.5, D = 0.5 and C_a = 220 nF that are chosen above the diode rectifier output voltage can be determined to have an average value of approximately $V_{rec(avg)}$ = 250 V from $v_{rec,k}$ determined from the analysis, which is a triangular pulse train, then determine its average value. If the current of L_o is continuous V_o can be approximated as

$$V_o = \frac{D}{n} V_{rec(avg)} = \frac{0.5 * 250}{2.5} = 50 \tag{6.24}$$

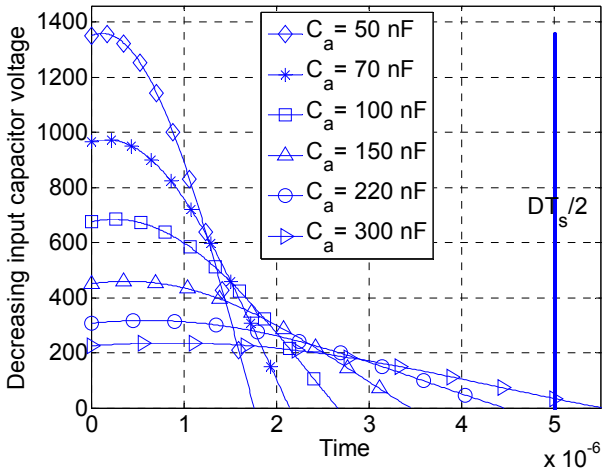
which is sufficiently close to the required V_o = 48 V, so that values of n, D and C_a can be set. The converter's operation with these values and its ability to satisfy the regulatory standards must be confirmed with a "check" stated at the end of the design procedure.



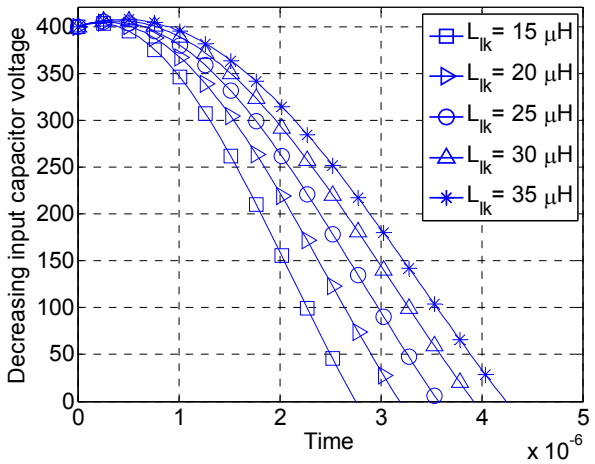
(a). Effect of varying C_a on charging time of C_a – n = 2.5, D = 0.5 and P_o = 1.92 kW.



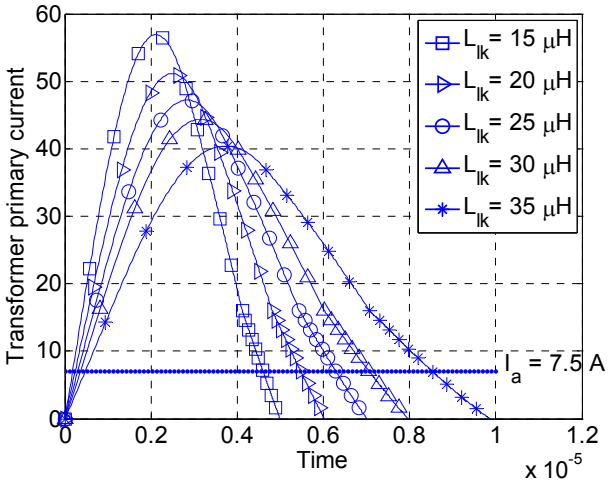
(b). Effect of varying C_a on discharging time of C_a–n = 2.5,D = 0.5 and P_o = 1.92 kW.



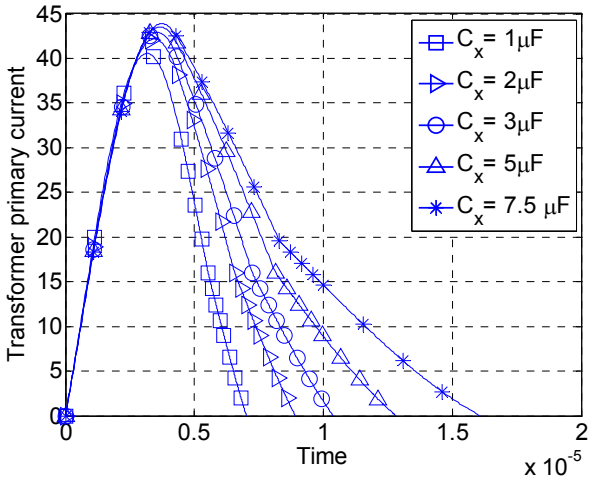
(c). Effect of varying C_a on discharging time of C_a-n = 2.5, D = 0.25 and P_o = 0.96 kW.



(d). Effect of varying L_{lk} on discharging time of C_a-n =2.5, D = 0.5 and C_a = 220 nF



(e). Effect of varying L_{lk} on decreasing i_{Llk}-n = 2.5, D = 0.5, C_a = 220 nF and C_x = 3μF



(f). Effect of varying C_x on decreasing i_{Llk}-n = 2.5, D = 0.5, C_a = 220nF, L_{lk} = 35 μH.

Fig 6.5: Design curves.

6.4.3 Determination of Leakage Inductance L_{lk} and Auxiliary Capacitor C_x

The values of L_{lk} and C_x are critical parameters that affect the auxiliary circuit's ability to reduce transformer primary current. In addition to its impact on the auxiliary circuit, L_{lk} also affects the $v_{Ca,k}$ waveform because there is a direct resonant interaction between L_{lk} and C_a when C_a discharges. The smaller L_{lk} is, the quicker C_a discharges as the resonant cycle is reduced; however, $i_{Llk,k}$ also decreases faster due to the counter voltage that is placed on L_{lk} by C_x.

If $i_{Llk,k}$ drops to a level that is less than the current coming out of the diode bridge rectifier ($i_{bus,k}$) and switch S_1 (or S_4) has not been turned off by the end of Mode 3, then C_a will begin to charge prematurely by part of $I_{a,k}$ before it has been fully discharged. If C_a is not fully discharged, then low frequency harmonics may be introduced into $I_{a,k}$.

L_{lk} should not be too large, however, as this will slow down the rate of decrease of $i_{Llk,k}$ too much when the converter is in a freewheeling mode of operation. Since $i_{Llk,k}$ must ideally be dropped to zero before the converter exits this mode and enters a power transfer mode, this means that the amount of time allowed for a freewheeling mode to occur must be increased so that the current can be extinguished. Doing so, however, limits D, and then the converter will not be able to provide the required V_o.

C_x is a critical parameter because it sets the counter voltage that is available to extinguish $i_{Llk,k}$ and it helps determine the minimum duration of the freewheeling modes of operation. If C_x is too small, it will not have enough energy in it to discharge L_{lk} during the freewheeling mode, thus $i_{Llk,k}$ will not be properly extinguished. However, if C_x is selected to be too large, unnecessary conduction will reduce the overall efficiency.

For this step, what needs to be done is (i) determine a range of acceptable values of L_{lk} that prevents C_a from prematurely charging (Fig. 6.5(d)), and (ii) look at values of C_x using these values of L_{lk} to find appropriate values of C_x and L_{lk} so that $i_{Llk,}$ is

extinguished by the end of the freewheeling mode (Figs. 6.5(e) and (f)). Fig. 6.5(d) is a graph of decreasing input capacitor voltage curves versus time for $D = 0.5$, $n = 2.5$, and instantaneous input current $I_{a(pk)} = 7.5$A; the graph shows how the discharging time of C_a is affected by the L_{lk} (15 μH ≤ L_{lk} ≤ 35 μH). All the curves shown in Fig. 6.5(d) start with a voltage of 400 V at time $t = 0$ because, as can be seen from Fig. 6.5(a), $V_{Ca(pk)} =$ 400 V when $C_a = 220$ nF.

It can be seen from Fig. 6.5(d) that it takes about 4.25 μs for $v_{Ca,k}$ to become zero when $L_{lk} = 35$ μH, which is the maximum value within the range of possible values of L_{lk}. If L_{lk} is reduced, however, then C_a will discharge faster, as can be seen in Fig. 6.5(d). Once $v_{rec,k} = 0$, $i_{Llk,k}$ decreases due to the counter voltage impressed across L_{lk}. After $i_{Llk,k} <$ $I_{a,k}$, C_a will start to charge again unless S_1 (or S_4) is turned off by that time; premature charging can distort the line currents.

Fig. 6.5(e) is a plot of curves of $i_{Llk,k}$ vs. time for different L_{lk} values. The time $i_{Llk,k}$ reaches its peak value corresponds to the time when $v_{Ca,k} = 0$ and energy that was stored in the input capacitors is transferred to L_{lk}. If $L_{lk} = 35$ μH then according to Fig. 6.5(e) $i_{Llk,k}$ takes around $\Delta t = 9$ μs from $t = t_0$ for $i_{Llk,k} = 7.5$ A (= $I_{a(pk)}$). If L_{lk} is reduced, then Δt is reduced considerably, which increases the probability for premature charging. As Δt for $L_{lk} = 35$ μH is close to the duration of the power transfer mode ($DT_s/2 = 10$ μs), there is little opportunity for the premature charging of C_a to occur.

Fig. 6.5(f) shows a graph of $i_{Llk,k}$ versus time for various values of C_x with $L_{lk} = 35$ μH, from which the time needed to extinguish the maximum transformer current ($I_{Llk(pk)}$) can be seen; If a value of $C_x = 3$ μF is chosen, then it can be seen from the graph that $i_{Llk,k}$ is ideally extinguished between 10 μs and 20 μs from the start of Mode 1. The selected L_{lk}–C_x combination determines the switch current stress $I_{Llk(pk)} = 40$ A.

6.4.4 Determination of Input Inductors $L_a = L_b = L_c$

Determination of the input inductors for Converter #2 is same as it was for Converter #1; thus it is not repeated here. If the reader needs more information please refer to Section 5.5.4 of Chapter 5.

6.5 Experimental Results of Converter #2

An experimental prototype of Converter #2 was built to confirm its feasibility. It was built for same specification stated above which is same as for Converter #1. The prototype was designed using, IXGH50N90B2D1 devices as the switches, DSI45–16A–ND devices as the three–phase AC–DC rectifier diodes and FFA40UP35STU–ND devices as output side diodes. Typical converter waveforms are shown in Figs. 6.6–6.10. Fig. 6.6 shows the phase current and phase voltage for different load conditions from 1.92 kW to 400W.

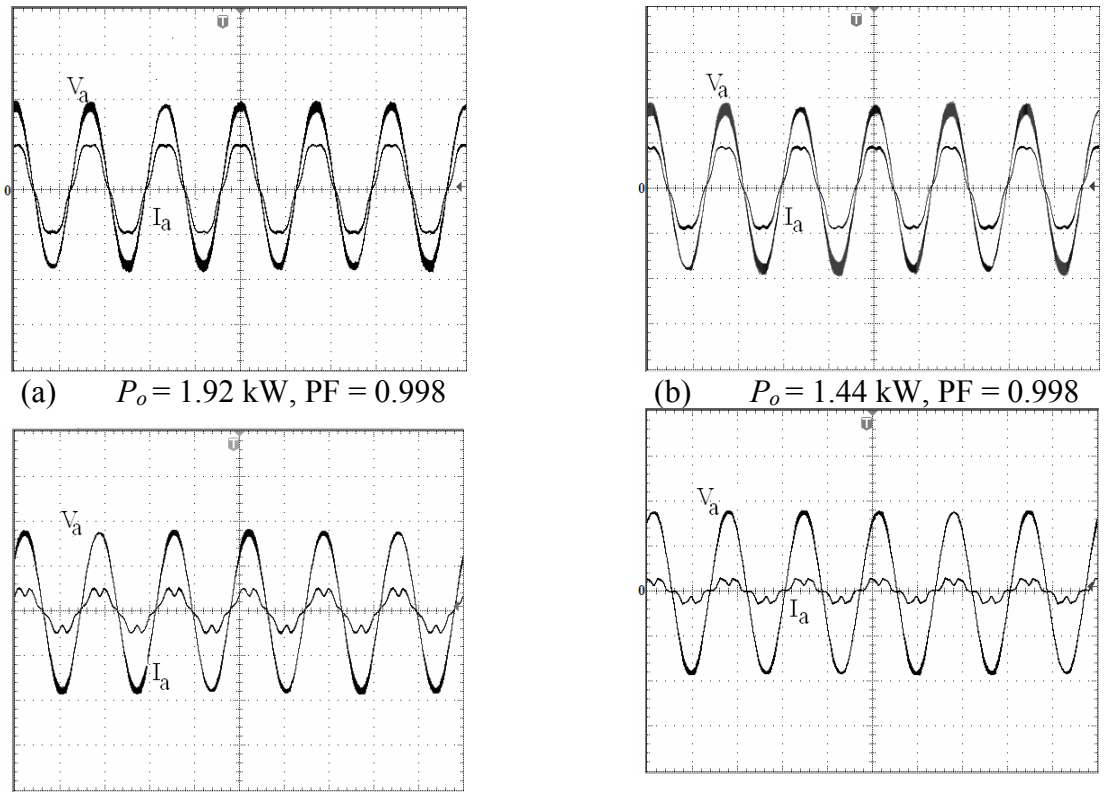
It can be seen from Fig. 6.6 that the converter can operate with near sinusoidal input currents from full load until half load (Figs. 6.6 (a) and 6.6 (b)) and then they start to become distorted; however, their harmonic content can still meet the IEC 61000–3–2 class A as shown in Table 6.1. It can also be seen that the input current becomes more sinusoidal as the load is increased so that the worst–case harmonic content occurs under light load conditions.

Figs. 6.7(a) and 6.8 show that voltage across an input capacitor when the converter is working with full load and with different time scales. It can be seen that this voltage is discontinuous, as it must be in order for a nearly sinusoidal input current waveform to be achieved.

Fig. 6.9 (a) and (b) shows the voltage and current waveforms of a switch in the leading leg at 1.92 kW and 400W respectively. The figures demonstrate that switch current is negative (body diode conducts) when the switch voltage becomes zero. Fig. 6.10 (a) and

Table 6.1: IEC 61000–3–2 Class A standard limits (rms), harmonics (rms) of phase current for loads 1.92 kW – 400W and PF.

Harmonics	Class A	1.92 kW	1.44 kW	0.96 kW	400 W
5^{th}	2.06	0.221	0.117	0.267	0.260
7^{th}	1.39	0.028	0.051	0.132	0.042
11^{th}	0.60	0.014	0.013	0.035	0.047
13^{th}	0.38	0.017	0.011	0.023	0.037
PF	–	0.998	0.998	0.983	0.95



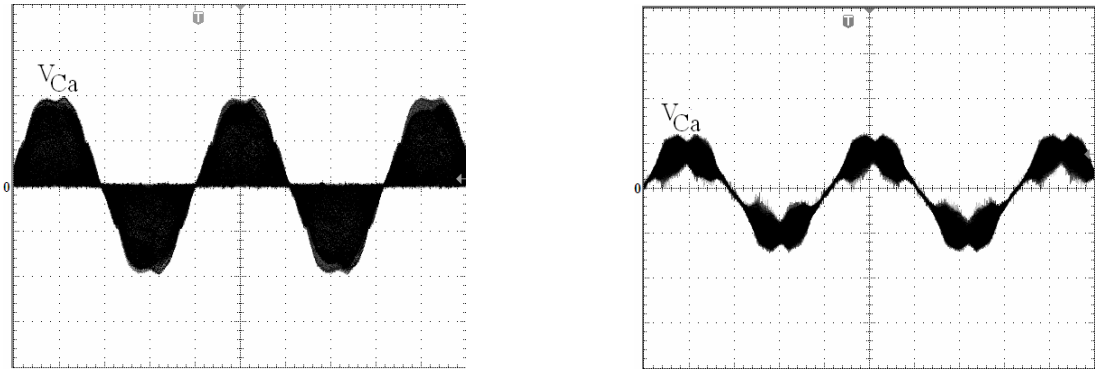
(a) P_o = 1.92 kW, PF = 0.998 (b) P_o = 1.44 kW, PF = 0.998

(c) P_o = 0.96 kW, PF = 0.983 (d) P_o = 400 W, PF = 0.95

Fig 6.6: Phase voltage and phase current (V_a = 100 V/div, I_a = 7.5 A/div, t = 10 ms/div).

(b) shows the voltage and current waveforms of a switch in the lagging or leg at 1.92 kW and 400W respectively. It can be seen how the primary transformer current is extinguished and the current in the lagging leg switch drops to nearly zero before the switch is turned off.

Table 6.2 presents a detailed comparison of Converter # 1 (Fig. 6.1) and Converter # 2 (Fig. 6.2). As explained in the Table 6.2, Converter #1 has better peak switch current stress, output current ripple and hold–up time while Converter #2 has better peak switch voltage stress, input power factor and efficiency. With respect to efficiency, it should be noted that no soft–switching techniques or energy recovery circuits were used to improve efficiency as it was desired to maintain the focus of the chapter on investigating the properties and characteristics of the two converters, as was done in Chapter 5.



(a) (b)

Fig 6.7: Input capacitor phase voltage for P_o = (a) 1.92 kW, (b) 400 W (V_{Ca} = 200 V/div, t = 4 ms/div).

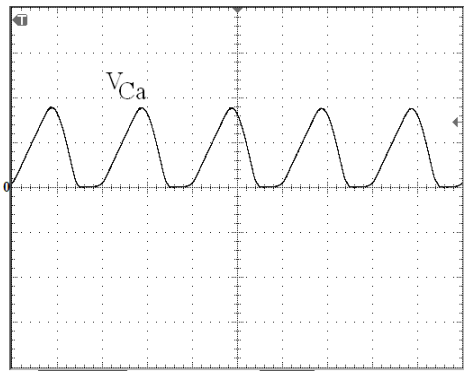
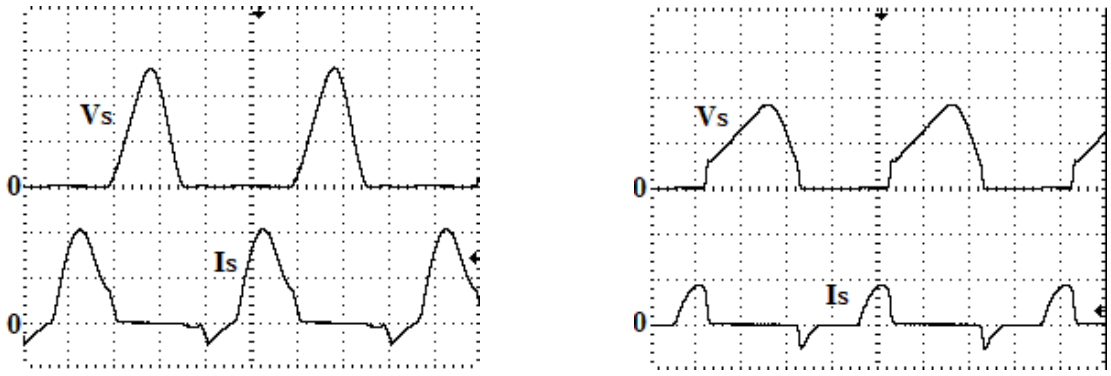
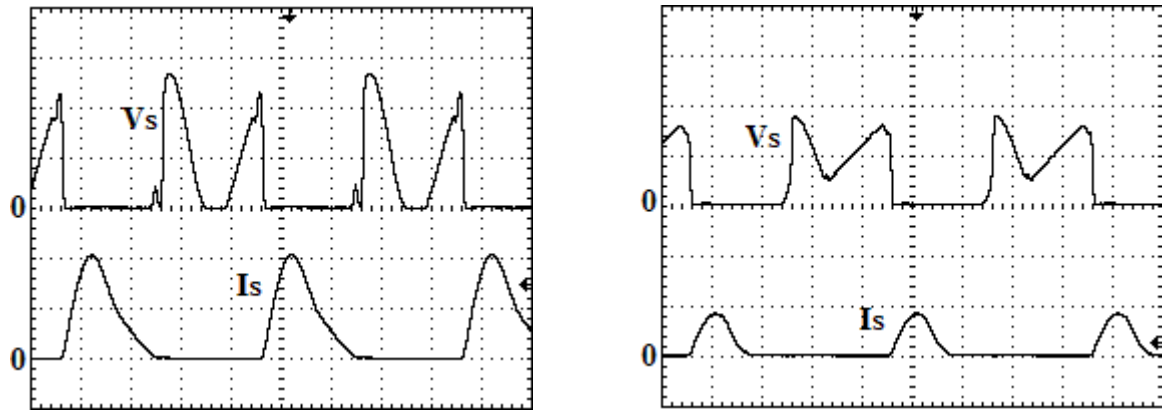


Fig 6.8: Input capacitor phase voltage when P_o = 1.92 kW (V_{Ca} = 200 V/div, t = 10 μs/div).



(a) (b)

Fig 6.9: Voltage and current of the leading leg switch when, P_o = (a) 1.92 kW and (b) 400 W (V_s = 300 V/div, I_s = 20 A/div, t = 10 µs/div).



(a) (b)

Fig 6.10: Voltage and current of the lagging leg switch when, P_o = (a) 1.92 kW, (b) 400 W (V_s = 300 V/div, I_s = 20 A/div, t = 10 µs/div).

6.6 Features of Single-Stage Full-Bridge Type Converters

6.6.1 Converter # 1

A. Peak Switch Current Stress

The switches in Converter #2 can be directly exposed to the sum of the current coming from the input inductors and the discharging current of the input capacitors. The switches

in Converter #1 are only exposed to the current coming out of the DC bus capacitor. Since the current that comes out of the diode bridge rectifier has peaks that the current that comes of the DC bus capacitor of Converter #1 does not, the peak switch current stress of the switches in Converter #2 is greater than that of the switches in Converter #1. From the experimental prototypes, it was found that the peak switch current stress for Converter #1 was approximately 30 A while that for Converter #2 was approximately 40 A.

B. Output Ripple

Converter #1 has a bulk capacitor across its DC bus that Converter #2 does not have. Even though this capacitor is disengaged from the bus whenever the converter enters a freewheeling mode, nonetheless, it helps to filter out the low 360 Hz component that is contained in the front–end bridge rectifier output voltage. As a result, this component is not present in the output of the converter as it is for Converter #2. This 360 Hz ripple can be removed from Converter #2 if bulkier filtering is used at its output.

C. Hold–Up Time

The presence of a bulk capacitor in Converter #1 means that the Converter #1as hold–up time capability if needed. Hold–up time is defined as the amount of time that a converter can provide the required output after the input AC voltage has been lost and may be needed if the converter is operating in a power system without battery back–up. In the case of Converter #1, energy stored from C_{bus} can help maintain the required output voltage in the case of a loss of input AC voltage, whereas Converter #2 cannot do so because it does not have a bulk capacitor.

6.6.2 Converter # 2

A. Peak Switch Voltage Stress

The switches in Converter #2 can have lower peak switch voltage stress than those of Converter #1. This is because the peak switch voltage stress of Converter #1 is the sum of the output voltage of the front–end diode bridge rectifier and the voltage across the DC bus

capacitor C_{bus} while the peak switch voltage stress of Converter #2 is equal to just that of the diode bridge rectifier output voltage. From the experimental prototypes, it was found that the peak switch voltage stress for Converter #2 was approximately 700 V while that for Converter #1 was approximately 1000 V.

B. Input Power Factor

The ability of both converters to provide sinusoidal input currents with minimal distortion is dependent on the ability of their input capacitors to operate with fully discontinuous voltages through the input line cycle. The smaller the input capacitor value is, the quicker these capacitors can discharge, increasing the likelihood of fully discontinuous voltage operation. Decreasing the input capacitor value, however, increases the peak voltage across a capacitor, which in turn, increases the peak voltage stress of the converter's switches. There is, therefore, a compromise that must be made between input power factor and peak switch voltage stress.

In the case of Converter #2, it is easier to make this compromise as it has, inherently, less switch peak voltage stress than Converter #1 so that Converter #2 can be made to operate with a better input power factor than Converter #1. The input power factor of the two converters, as obtained from the experimental prototypes, is shown in Table. 1 for various loads.

C. Efficiency

Converter #2 has a direct path of power transfer from the output of the front–end bridge rectifier to the input of the full–bridge. In Converter #1, energy must be transferred from the converter's input section to its DC bus section before it is transferred to its full–bridge section. Moreover, Converter #1 has current that freewheels in the DC bus that Converter #2 does not when the converters are in a freewheeling mode of operation. As a result, Converter #2 is more efficient than Converter #1. From the experimental prototypes, it was found that Converter #2 had a maximum efficiency of 83% that Converter #1 had a maximum efficiency of 80% and that Converter #2 was approximately 2.5% – 3% more efficient throughout the load range.

6.7 Conclusion

This chapter is a continuation of the work discussed in the previous chapter as its main focus of the chapter is a comparison of converter presented in Chapter 5 (Converter #1) with a modified version of it (Converter #2). The main difference between the two converters is that the modified converter does not have a bulk capacitor in its DC bus. In the chapter, the modes of operation of the modified converter were explained in detail and a procedure for the design of this converter was demonstrated with an example. Experimental results obtained from a prototype of the modified converter were presented and based on these results; the two converters were compared in terms of parameters such as input power factor and efficiency. It was determined that the original converter (Converter #1) has better peak switch current stress, output current ripple and hold–up time while the modified converter (Converter #2) has better peak switch voltage stress, input power factor and efficiency.

Chapter 7

7 Conclusion

7.1 Introduction

In this chapter, the contents of the thesis are summarized, conclusions resulting from the thesis work are presented, the contributions of the thesis to the power electronics literature are stated, and suggestions for future work are given.

7.2 Summary

The main focus of this thesis has been the investigation of new power converter topologies that convert a three-phase AC input voltage into an isolated DC output voltage. Conventional three-phase AC-DC converters have two converter stages. They have a front-end converter that converts the input AC voltage into an intermediate DC bus voltage and a second, back-end converter that converts this DC bus voltage into the desired isolated DC output voltage. The front-end converter also performs power factor correction (PFC) and shapes the three-phase input currents so that they are nearly sinusoidal and in phase with the three-phase input voltages. This allows the AC power source to be used in the most efficient manner.

The front-end AC-DC converter is typically with six switches while the back-end DC-DC converter is typically implemented with a four switch DC-DC full-bridge topology. Power electronic researchers have been motivated to try to reduce the number of switches that are used in the conventional two-stage approach in order to reduce cost and simplify the overall AC-DC converter. There are two general approaches to doing this: The first approach is to reduce the number of switches in the front-end AC-DC converter. The second approach is to combine the AC-DC converter and the DC-DC converter in a single converter so that the overall AC-DC converter can be implemented in a single converter stage that can simultaneously perform AC-DC power conversion with PFC and DC-DC power conversion.

The contents of this thesis can be summarized as follows:

In Chapter 1, certain basic concepts relating to the main focus of the thesis were introduced, the relevant literature was reviewed, and the thesis objectives and outline were stated.

In Chapter 2, it was explained how the three-phase AC-DC front-end converter of a two-stage AC-DC converter can be implemented with just one switch, in topologies that are based on the six fundamental non-isolated DC-DC converters: Boost, Ćuk, Sepic, Buck, Buck-Boost and Zeta. The first three converters being converters with inductive input filters and the others being converters with capacitive input filters, when implemented as a DC front-end converters. It was explained how the switch in these three-phase single-switch front-end converter is subjected to a high peak voltage stress, which makes them impractical for most industrial applications. It was also explained how the peak voltage stress of this switch can be reduced if a single-switch structure is replaced by a two-switch multilevel structure so that none of the two switches is exposed to the high peak voltage that the single switch is.

Two types of front-end multilevel converters were identified. The first was the "flying-capacitor" type, which is based on conventional multilevel structures found in high voltage DC-AC inverters. Three-phase flying-capacitor front-end AC-DC multilevel converters that were based on each of the six fundamental non-isolated DC-DC converters were presented and it was explained that the main drawback of the flying capacitor converters was the unequal peak voltage stresses. As a result, a new family of three-phase front-end AC-DC multilevel converters that was based on the connection of a neutral-point of a three-phase input capacitor filter to the general DC-DC structure embedded in the front-end converter was proposed. Examples of how a new Ćuk neutral-point connected front-end AC-DC multilevel converter (example of an inductive input filter converter) and a new buck-boost neutral-point connected front-end AC-DC multilevel converter could be synthesized were presented.

In Chapter 3, the operation of the new buck-boost neutral-point connected front-end AC-DC multilevel converter was investigated in detail as an example of a new neutral-point connected multilevel converter. The buck-boost converter was considered for

further study as it was the simplest converter, with respect to the Ćuk, Sepic and Zeta converters, that can both step up and step down input voltage and the properties of a reduced switch converter that can do both have not been examined in the literature. The chapter began with an in-depth explanation of the converter's modes of operation, followed by a statement of its features. A mathematical analysis of its key steady-state characteristics was then presented and the results of this analysis were used to generate graphs of steady-state characteristics curves. These graphs were used to develop a procedure for the design of key component values and the procedure was demonstrated with a design example. The results of the design example were used to implement a converter prototype that was used to confirm the feasibility of the new AC-DC buck-boost converter and to determine the characteristics of this new converter. Experimental results that were used in this confirmation were presented in the chapter.

A variation of the buck-boost converter investigated in Chapter 3 was presented in Chapter 4. This converter was implemented with a quasi-resonant technique to reduce switching losses by shaping the current through each switch so that it is forced the switch current to be zero when it is turned on and forced to eventually return to zero some time before it is turned off. Since switching losses are dependent on the product of switch voltage and switch current at the time of a switching transition (from off to on and vice versa), the quasi-resonant technique can significantly reduce turn-on and turn-off switching losses.

Similar to the buck-boost front-end converter presented in Chapter 3, the operation of the new buck-boost quasi-resonant neutral-point connected front-end AC-DC multilevel converter was investigated in detail. The converter's modes of operation were explained in detail, its features were stated, a mathematical analysis of its key steady-state characteristics was performed, and the results of this analysis were used to generate graphs of steady-state characteristics curves that were used to develop a procedure for the design of key component values. The procedure was demonstrated with a design example and the results of the example were used to implement a converter prototype. Experimental results that confirmed the feasibility of the new quasi-resonant buck-boost converter were presented at the end of the chapter.

In Chapter 5, the second approach to reducing the number of switches typically found in conventional two-stage AC-DC converters – the use of single-stage converters that combine the two converter stages of the conventional approach into one converter – was examined. A new AC-DC single-stage converter was introduced in this chapter. This converter combined an AC-DC buck front-end converter with a DC-DC full-bridge converter in a single topology. In this chapter, the basic fundamental principles of this converter were explained, the converter modes of operation were presented and its features were stated. A mathematical analysis of the converter's steady-state characteristics was performed, a design procedure was developed using the results of this analysis, and the procedure was demonstrated with an example that was used to design and implement a prototype converter, from which experimental results were obtained.

In Chapter 6, a variation of the converter that was investigated in Chapter 5 was presented. The main difference between the two converters was that this converter (called Converter #1) did not have a bulk capacitor connected to its intermediate DC bus as did the converter in Chapter 5 (called Converter #2). This new converter, Converter #1, was examined, analyzed, designed and implemented in the same manner as the previous converter, Converter #2, and the performance and characteristics of the two converters were compared.

7.3 Conclusions

The following conclusions can be made based on the work performed in this thesis:

i. It is possible to synthesize a three-level, AC-DC, neutral-point connected, multilevel two-switch front-end converter for each of the six fundamental three-phase single-switch AC-DC converters. It was confirmed by computer simulation that each of these new converters can work and can allow both converter switches to each have the same peak voltage stress, which is not the case for the flying-capacitor multilevel converters, which have uneven peak voltage stresses.
ii. The new neutral-point connected buck-boost converter can step up voltage (boost mode) and can step down voltage (buck mode). It was determined that input power factor was better when the converter is operated in buck mode of operation than in

boost mode because there is more current available to discharge the input capacitors before the end of each switching cycle – discontinuous input capacitor voltages being the key to ensure a good input power factor.

iii. It was determined that the above buck-boost converter can operate with greater efficiency when it is boost mode than in buck mode because the circulating current is less in boost mode with respect to buck mode; thus conduction losses are low.

iv. The quasi-resonant neutral-point connected converter can operate with zero-current switching (ZCS), but with less efficiency than the neutral-point connected buck-boost converter for the load range considered in this thesis, a maximum of approximately 2 kW. This is because the quasi-resonant converter has significant conduction losses that are caused by the additional circuitry that is used to shape the switch current to ensure that the switches operate with ZCS. The conduction losses offset the switching losses that are eliminated by the quasi-resonant technique. Although it has been shown in the literature that quasi-resonant converters can be used for higher power applications (up to 6 kW) than converters without quasi-resonant, this could not be confirmed with the available laboratory facilities because with available facilities the maximum obtainable power is 2 kW.

v. The quasi-resonant neutral-point connected converter can operate with a better input power factor than the buck-boost converter presented in Chapter 3. This is because due to resonance between additional LC components more circulating current is created in the DC side; thus input capacitors are forced to discharge irrespective of the load or. Also QR buck-boost converter is operated with variable switching frequency, as a result switch off time is adjusted based on the load so that input capacitor voltages will be fully discontinuous and bounded by the sinusoidal envelope.

vi. Comparison of two buck-type three-phase, single-stage, AC-DC full-bridge converters – Converters #1 and #2 - was presented in Chapter 6. They can be considered to be the dual of the fundamental three-phase single-stage boost converter. These basic converters are simple and can operate with an excellent input power factor using standard phase shift PWM control. In the chapter, the operation of Converters #1 was explained with the equivalent circuit diagrams and

the typical waveforms, experimental results that were obtained from prototype was presented, and a detailed comparison between the two topologies was made.

vii. Converter #1 was found to have a lower switch voltage stress, a better input power factor and efficiency, and Converter #2 was found to have a lower current stress, inherent filtering of low frequency output harmonics, and hold-up capability. This comparison was summarized at the end of the chapter.

7.4 Contributions

The main contributions of this thesis to the power electronics literature are as follows:

i. A new family of three-phase AC-DC multilevel converters that can be used as the front-end converter of a two-stage AC-DC converter was introduced.
ii. It was shown how the converters from the new family can be synthesized from three-phase single-switch AC-DC front-end converters.
iii. The steady-state properties and characteristics of one of the converters from this new family, the buck-boost converter, were determined based on a detailed investigation involving mathematical analysis and experimental verifications.
iv. A new quasi-resonant buck-boost multilevel front-end converter was introduced and its steady-state properties and characteristics were determined.
v. Two new three-phase AC-DC single-stage converters were presented and examined in detail and the characteristics of these converters were compared.
vi. In total, four new three-phase converters – two new AC-DC front-end converters for two-stage converters and two new AC-DC single-stage converters – were presented in this thesis. For each of these converters, a procedure for the selection of key converter components was developed and its operation was confirmed with experimental results.

7.5 Future Work

The following future work can be performed:

i. It was found that the quasi-resonant neutral-point connected multilevel buck-boost converter had lower efficiency with the quasi-resonant technique than without for the maximum load range of up to approximately 2 kW. Future work can be performed to see how the quasi-resonant converter operates with higher loads. It is expected that the quasi-resonant converter will have the higher efficiency, but this needs to be confirmed.

ii. The main objective of the research on the two single-stage converters that were presented in Chapters 5 and 6 was to investigate their properties and characteristics. Such an investigation has rarely been done and the investigation itself represents a significant contribution to the power electronics literature. The efficiency of the two converters, however, was low and this was mainly due to the fact that soft-switching techniques that can make either the switch voltage or switch current zero during switching transitions were not used. Future work can be performed to see what effect that implementing the single-stage converters presented in this paper with efficiency improving soft-switching techniques would have on their performance.

iii. Multilevel level topologies allow their switches to operate with lower peak voltage stresses than two-level topologies. The single-stage converters presented in Chapters 5 and 6 had high peak voltage switch stresses because they were not multilevel topologies, unlike those of the new front-end converters presented in Chapters 2 to 4. Future research can be done to see if the two new single-stage converters can be implemented with multilevel topologies.

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